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SURFACE ACOUSTIC WAVE MICROWAVE OSCILLATOR AND FREQUENCY SYNTHE--ETC(U)
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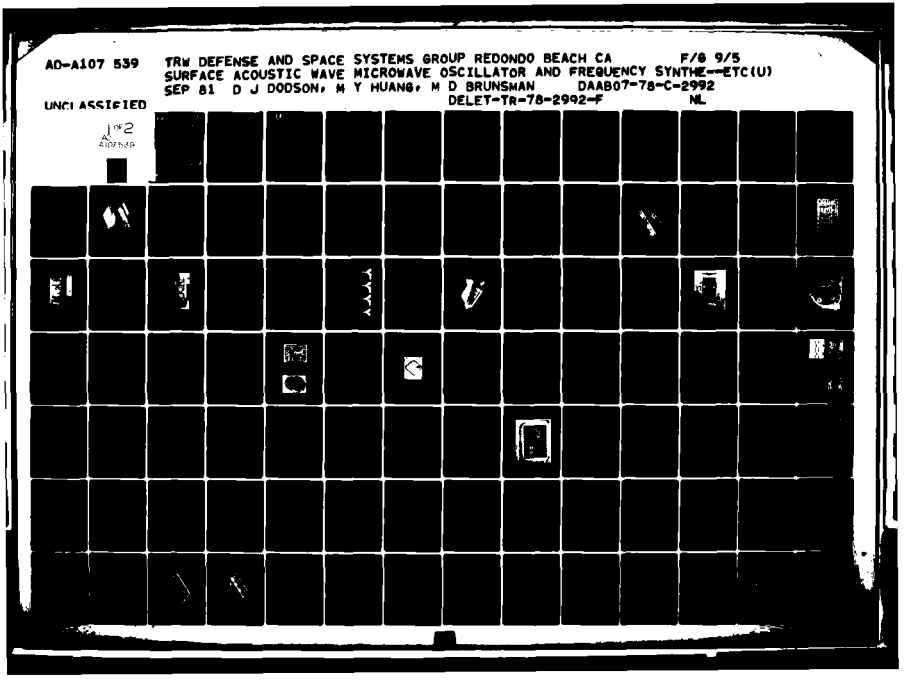

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LEVEL II

Research and Development Technical Report

DELET-TR-78-2992-F

SURFACE ACOUSTIC WAVE MICROWAVE OSCILLATOR AND FREQUENCY SYNTHESIZER

D.J. Dodson, M.Y. Huang, M.D. Brunsman
TRW Inc.
One Space Park
Redondo Beach, CA 90278

September 1981

Final Report for Period 1 October 1979 - 31 March 1981

Prepared for:
ELECTRONICS TECHNOLOGY & DEVICES LABORATORY

ERADCOM

US ARMY ELECTRONICS RESEARCH AND DEVELOPMENT COMMAND
FORT MONMOUTH, NEW JERSEY 07703

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This final report details the technical progress achieved on task II of the program Surface Acoustic Wave Microwave Oscillator and Frequency Synthesizer. The objective of the Task II effort was to establish a synthesizer design which, when packaged, provided a significant reduction in size, weight and power consumption as compared with current direct synthesis techniques. The hardware implementation was to highlight Surface Acoustic Wave (SAW) device applications specifically geared toward addressing performance parameters.

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such as switching speed, frequency step size, and total achievable bandwidth, as well as maximum suppression of spurious modes. The approach chosen was to incorporate SAW devices as oscillators and delay lines/filters, together with monolithic large scale integrated circuits which work at RF frequencies (RF-LSI) in an iterative mix-and-divide architecture. To this end, a brassboard synthesizer has been fabricated and delivered. At program completion, the brassboard unit is fully operational and has been tested in order to characterize typical unit performance capabilities. The delivered synthesizer demonstrated outstanding switching speed, settling in less than 25 ns and provided an output whose phase noise was measured to be within the specified requirements, as measured to within 2 MHz of the carrier at an output frequency of 1308 MHz. Output spectral flatness was obtainable to within ± 1.2 dB over the operational band, with achievable output power greater than +10 dBm.

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1.0 OVERVIEW

This final report details the technical progress of Program DAAB07-78-C-2992, Surface Acoustic Wave Microwave Oscillator and Frequency Synthesizer. In particular, this report concludes the efforts undertaken in fulfillment of Task II of the contract; the design of a SAW based microwave frequency synthesizer. The specific objective of the Task II effort was to establish a synthesizer design which, when packaged, provided a significant reduction in size, weight, and power consumption as compared with current direct synthesis techniques. The hardware implementation was to highlight Surface Acoustic Wave (SAW) device applications specifically geared toward addressing performance parameters such as switching speed, frequency step size, and total achievable bandwidth, as well as maximum suppression of spurious modes. TRW's approach to this synthesizer design was to incorporate SAW devices in the oscillator and filter circuits and use monolithic large scale integrated circuits which work at RF frequencies (RF-LSI) in an iterative mix-and-divide architecture as shown in the diagram of Figure 1-1. To this end, a brassboard synthesizer has been fabricated and delivered. At program completion, the brassboard unit is fully operational and has been tested in order to characterize typical unit performance capabilities. The delivered synthesizer demonstrated outstanding switching speed, settling in less than 25 ns and provided an output whose phase noise was measured to be within the specified requirement, as measured to within 2 MHz of the carrier at an output frequency of 1308 MHz. Output spectral flatness obtained was to within $\pm$1.2 dB over the operational band, with achievable output power greater than +10 dBm. Figure 1-2 shows the completed single output deliverable synthesizer configuration.

As shown in the block diagram, the synthesizer design incorporates three functional modules:

1) Tone generation module with oscillator fundamental frequencies of 486, 526.5, 567, and 607.5 MHz.
2) A synthesizer module
3) An output module

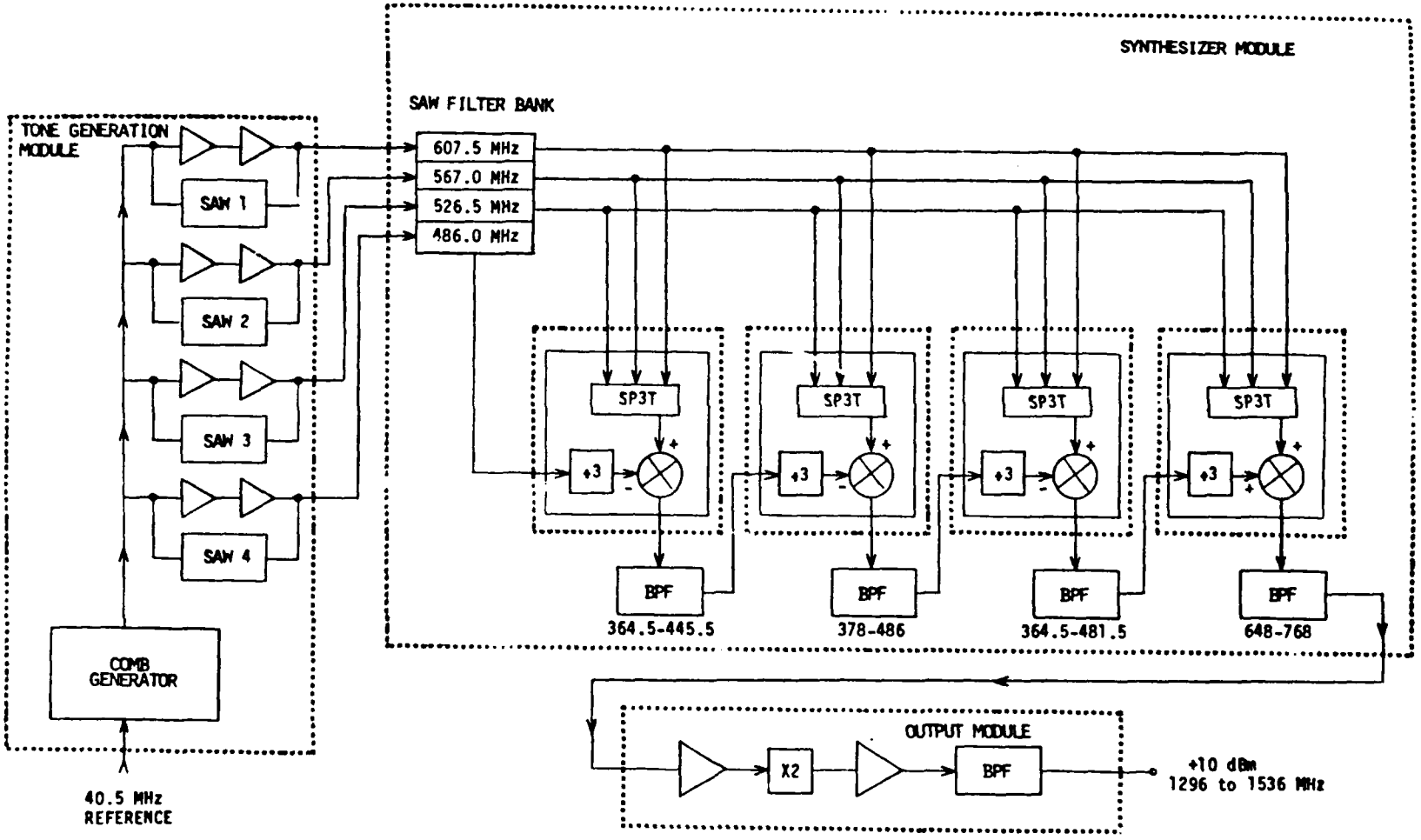


Figure 1-1. SYNTHESIZER WITH INDEPENDENT SAW OSCILLATORS

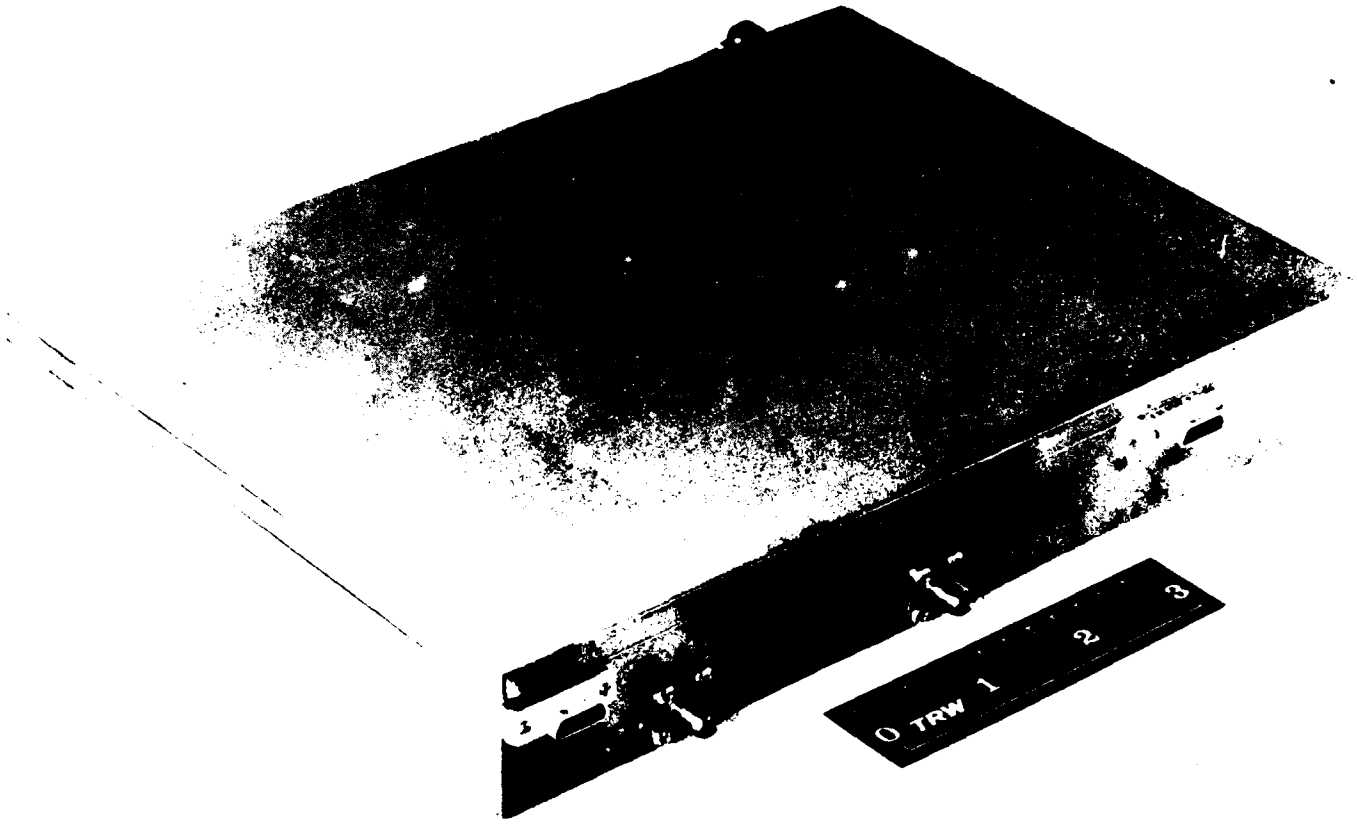


Figure 1-2. DELIVERABLE SYNTHESIZER CONFIGURATION

Placement of the single stage SAW filter bank in the synthesizer module functional block section of Figure 1-1 was done for the purpose of identifying the unique filtering function provided to the tone generation module outputs. However, input and output matching networks required for integration of the SAW filters with the tone generation module injection locked oscillator circuitry necessitated their close proximity to module (1) hardware. Further definition of the tone generation module (TGM) circuitry will be discussed in Section 3.3.

Deliverable versions of all three modules have been fabricated and tested, and their individual design-performance parameters will be discussed in detail in subsequent text.

2.0 SYNTHESIZER ARCHITECTURE

The synthesizer requirements studies conducted during the initial contract period established a systems architecture which would provide unit operation consistent with a majority of JTIDS Class 3 terminal hardware. The subsystem design philosophy proposed to implement the chosed hardware configuration was incorporated into a "modular" type of synthesizer configuration. The current synthesizer design is based on meeting the objectives set forth in the contract statement of work with the exception of the available output frequency range. We have provided for operation from 1296-1536 MHz, in conjunction with JTIDS Class 3 operation requirements. All other deviations from required performance shall be indicated in Section 5.0, subsection 5.8. Modifications to the initially proposed system designs were made in the frequency reference (comb generator/injection locked oscillator) and synthesizer module areas. In addition, circuitry has been added to provide voltage regulation and reference functions to the RF-LSI circuitry of the synthesizer module.

Two distinct frequency referencing schemes initially considered consisted of a dual PLL/multitone generation (MTG) technique and a multimode locked SAW oscillator design. Both approaches attempted to provide coherent synthesizer reference tones at 526.5, 567 and 607.5 MHz to the switch inputs from a single reference input frequency.

The dual PLL/multitone generator approach was accomplished by establishing simultaneous loop oscillations at 526.5 and 567 MHz, by way of redundant phase locked circuitry coherent with the 40.5 MHz reference input. Subsequent application of these tones to a nonlinear gain stage produced third order IM products, with 40.5 MHz spacings, in addition to the distinct 526.5 and 567 MHz tones at the MTG output. SAW filters with passbands centered at 526.5, 567 and 607.5 MHz following the multitone generation module would serve to attenuate the remainder of the unwanted "comb" spectra, thereby providing coherent reference frequencies to the switch inputs of the synthesizer module. The PLL/MTG concept was not incorporated in the final deliverable synthesizer due to its inherently large consumption of power and its lack of SAW technology utilization for generation of stable source tone frequencies.

The Multimode Locked SAW Oscillator (MLSO) technique was also proposed to generate the coherent tones required at the synthesizer module input. This implementation utilized a single PLL to generate a 486 MHz coherent input to a

multimode SAW oscillator from the 40.5 MHz reference input to the synthesizer. By utilizing a SAW delay line designed with multiple passbands at 526.5, 567, and 607.5 MHz in a saturated amplifier-loop technique, oscillation could be established at all three of the primary frequencies through the enhancement of IM products spaced at 40.5 MHz intervals of the PLL input frequency. The major difficulty with the MLSO approach was found to be in the desired injection locking properties of the output tones. Injection locking tests conducted on a breadboard MLSO indicated that simultaneous locking of all the desired output tones could not be achieved when the unit was driven from a single input frequency.

Since stability of the reference tones employing the MLSO approach could not be derived by injection locking at one of the desired output modes, the injection locked individual SAW oscillator approach was selected as the baseline reference circuitry configuration for the deliverable synthesizer. This approach consists of generating a comb of frequencies from the reference 40.5 MHz input. The comb is introduced to the inputs of each of four free-running SAW stabilized oscillators. Each of the oscillator loops is designed utilizing commercial wideband RF amplifier modules with SAW delay lines in the feedback path, thereby providing grossly centered tones about the 486, 526.5, 567 and 607.5 MHz center frequencies. Additional SAW bandpass filter elements are utilized at each oscillator output to filter adjacent tones, thereby providing attenuation of spurious components in compliance with the -68 dBc requirement.

Modifications to the synthesizer module hardware have been incorporated to insure the functional operation of the unit as proposed. Primarily, circuit design modifications were implemented to work around processing deficiencies in the RF-LSI ADM-1 circuitry. A detailed description of these modifications is given in Section 3.4.1.2.

2.1 Block Diagram

The block diagram in Figure 1-1 shows the basic structure and major building blocks of the baseline design. It provides 81 frequencies in 3 MHz steps from 1296 to 1536 MHz. This output implies a 320 MHz IF in the JTIDS terminal and may have to be modified to fit the specific needs of the JTIDS terminal design when one has been chosen.

The reference 40.5 MHz clock frequency is multiplied by the comb generator circuitry where enhancement of the 12th, 13th, 14th and 15th products at 486, 526.5, 567 and 607.5 MHz is achieved. This comb output spectrum, along with other 40.5 MHz spaced harmonics, is applied to the input of the four injection locked SAW oscillator networks. The coherent output tones of the injection locked oscillators are then filtered by the SAW bandpass filters to remove adjacent comb frequencies prior to application to the four RF-LSI building blocks of the synthesizer module. Each RF-LSI block is composed of an SP4T switch with driver, and an ADM-1 mix-and-divide chip.

Frequency synthesis is accomplished by selecting one of the three primary frequencies from the tone generator, by way of the SP4T RF-switch, and mixing this frequency with the divider reference frequency. The three primary frequencies are mixed through four stages to produce 81 (3^4) output frequencies. On the first ADM-1 chip, the selected frequency from the first SP4T switch is mixed with 162 MHz, which is derived by dividing the 486 MHz output of the tone generator module by a hardwired function of 3. Similarly, each of the three primary tones of the tone generator is selected as the RF port input to the ADM-1 mixer. In this fashion, each chip provides several possible output tones: the first outputs from 364.5 to 445.5 in 40.5 MHz steps; the second from 378 to 486 in 13.5 MHz steps; the third in 4.5 MHz steps from 364.5 to 481.5 MHz; and finally, 1.5 MHz steps are provided from 648 to 768 MHz. When this output is multiplied by 2, the desired 3 MHz steps from 1296 to 1536 MHz are generated by the output module. In addition, the output module provides output frequency flatness over the 1296-1536 MHz operating range and provides filtering of spurious tones generated outside of its 240 MHz bandwidth.

2.2 Module Specifications

The module specifications are delineated in Table 2-1. These values provide the key performance requirements and interfaces to assure a synthesizer that will meet the overall requirements.

Table 2-1. MODULE SPECIFICATIONS

Parameter	Comb Generator Module	Injection Locked Oscillators	Synthesizer Module	Output Module
f_{IN} (MHz)	40.5	486,526.5,567,607.5 (f_1-f_4)	486,526.5,567,607.5	648-768
P_{IN} (dBm)	+12.0	$\geq$-20 at f_1-f_4	-10 max; -14 min.	$\geq$-26
f_{OUT} (MHz)	486,526.5,567,607.5	Same	648-768 (1.5 MHz steps)	1296-1536 (3 MHz steps)
P_{OUT_1} (dBm)	$\geq$-20 at f_1-f_4	-10 max at 486 -14 min at 607.5	$\geq$-26	+10 $\pm$1.0
VSWR IN/OUT		$\leq$2:1	$\leq$2:1	$\leq$2:1
Spurious Level (dBc)		Locked: $\leq$-37 dBc	LO Feedthru: $\leq$-35 All Others: $\leq$-50	$\leq$-35
Switching Time (ns)			$\leq$30	
DC Power (W)	$\leq$ 5 mW	$\leq$ 6	$\leq$7.5	$\leq$3.75 @ 15V

3.0 HARDWARE DESIGN

The functional sections of the frequency synthesizer hardware can be broken down in a modular fashion to illustrate the associated operations encountered from input to output. Generation of the reference frequencies is accomplished in the comb generator and injection locked oscillator sections. Signal conditioning and processing of the reference frequencies is provided by hardware located in the SAW circuitry and synthesizer module sections. Final processing of the synthesizer module output is provided by the output module circuitry.

3.1 Control Box

In order to effectively evaluate several of the frequency synthesizer design capabilities, a stand-alone controller was built. This control box was designed to provide a fixed, as well as continuously variable, 8-bit TTL compatible control word to the four SP4T RF switches of the synthesizer. The control box provides for fixed frequency as well as swept and hopped mode synthesizer operation.

An externally-applied TTL-compatible control command is required at the synthesizer module SP4T switch word select pins to provide output frequency addressing. The 8-bit control word is applied to switch address pins 2^0 - 2^7 with address pin 2^7 representing the most significant bit (MSB), and address pin 2^0 signifying the lease significant bit (LSB). Internal routing of the command word connector harness to the synthesizer module switch select pin locations has been provided in such a manner so as to place the MSB at switch #4 (closest to output module) and the LSB at switch #1 (closest to the PLL/MTG circuitry) in reference Figure 1-1. Sequentially increasing output frequency operation is obtained by providing a modified digital word progression from 2^0 to 2^7 at the control word input to the synthesizer. By applying this modified sequential 8-bit binary word, from 00001000 to 10100010, a corresponding synthesizer output frequency range from 1296 to 1536 MHz is obtained. Swept mode of operation is obtained by stepping the "control word" through its 81 word states at a selectable rate. Hop mode operation is obtained by switching the word between two preset word addresses, at a selectable rate.

The control box serves as a tool by which output flatness and hop speed are easily obtained. Furthermore, the extended capabilities of the control box provide the user the ability to accurately determine synthesizer frequency settling time via external clock synchronization information.

3.1.1 Functional Capabilities

Aside from providing a fixed 8-bit word address to the frequency synthesizer, the control box capabilities allow the user to control the rate of change of the command word as well as the rate of change between two pre-selected start and stop frequency words.

The fixed mode of operation is selected by placing a front panel mode selector switch in the "single" operation position. In this mode, two front panel thumbwheel switches preset two possible single operating frequencies. An interconnected toggle switch then allows for selection of one of the two thumbwheel frequencies at any time.

Swept mode of operation is initiated by placing the front panel mode selector switch into the "sweep" position. Again the thumbwheel switches preset the start and end of sweep frequencies. Sweep clear and sweep reset momentary contact switches are provided for resetting and clearing previously selected sweep range frequencies. Swept operation can be obtained in an increasing frequency or decreasing frequency format simply by reversing the thumbwheel start-stop arrangement.

Hop mode of operation is obtained with the mode switch placed in the "hop" position. As before, the thumbwheel switches set the "hop from" and "hop to" frequency extremes. As in the sweep mode of operation, the hop mode is capable of providing for hopping from a higher to lower frequency as well as vise versa. This is accomplished by reversing the position of the thumbwheel switch word addresses.

Two front panel switches labeled "hop clock" and "sweep clock" are used to provide variable hop and sweep rates. These switches simply apply different time constant networks to each of the individual hop and sweep timing circuits. The hop rate is selectable from a rate of 0.2 Hz to a rate of 78 KHz, and the sweep rate obtainable ranges from 0.5 Hz to 2.55 KHz.

A detailed description of the timing circuitry and programmable counter design employed in the control box has been previously addressed, and will not be discussed at this point.

3.2 DC Board

Bias voltages required for the ADM-1 chip input amplifier and mixer circuitry are obtained from the +15 VDC and +5 VDC unregulated inputs. Output voltages of +10.0 VDC and +3.3 VDC are regulated by means of the circuitry shown in Figure 3-1 below. External pass transistors incorporating heat sinking are required in both regulators to insure safe operation at rated load over operating conditions. The deliverable DC board regulator circuitry is seen in Figure 3-2.

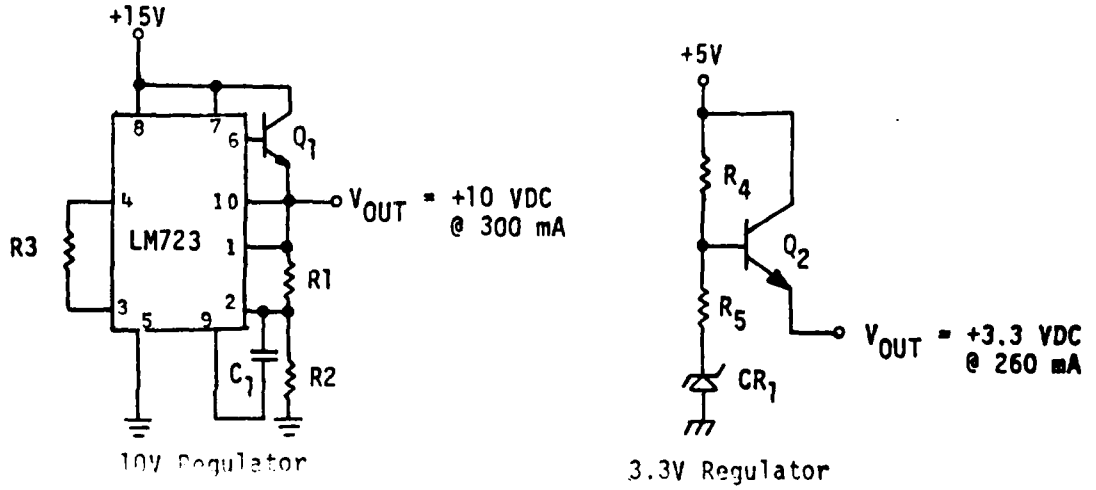


Figure 3-1. +10.0 VDC and +3.3 VDC REGULATOR CIRCUITRY

3.2.1 DC Board Requirements

The DC board +10V and +3.3V regulators provide biases at 300 mA and 260 mA rated loads, respectively, to the RF-LSI circuitry of the synthesizer module. The ADM-1 mix-and-divide device front end RF amplifiers require a +10V bias at 20 mA each. The mixer amplifier, A2, requires a +10V bias at 50 mA each, and the mixer requires a +3.3V bias at 55 mA each. Conservatively rating these loads, the above total bias currents are determined for each regulator (DC board), synthesizer module, utilizing a multiple-twisted-shielded cabling technique to minimize coupled RF signals in the upper slice of the synthesizer package.

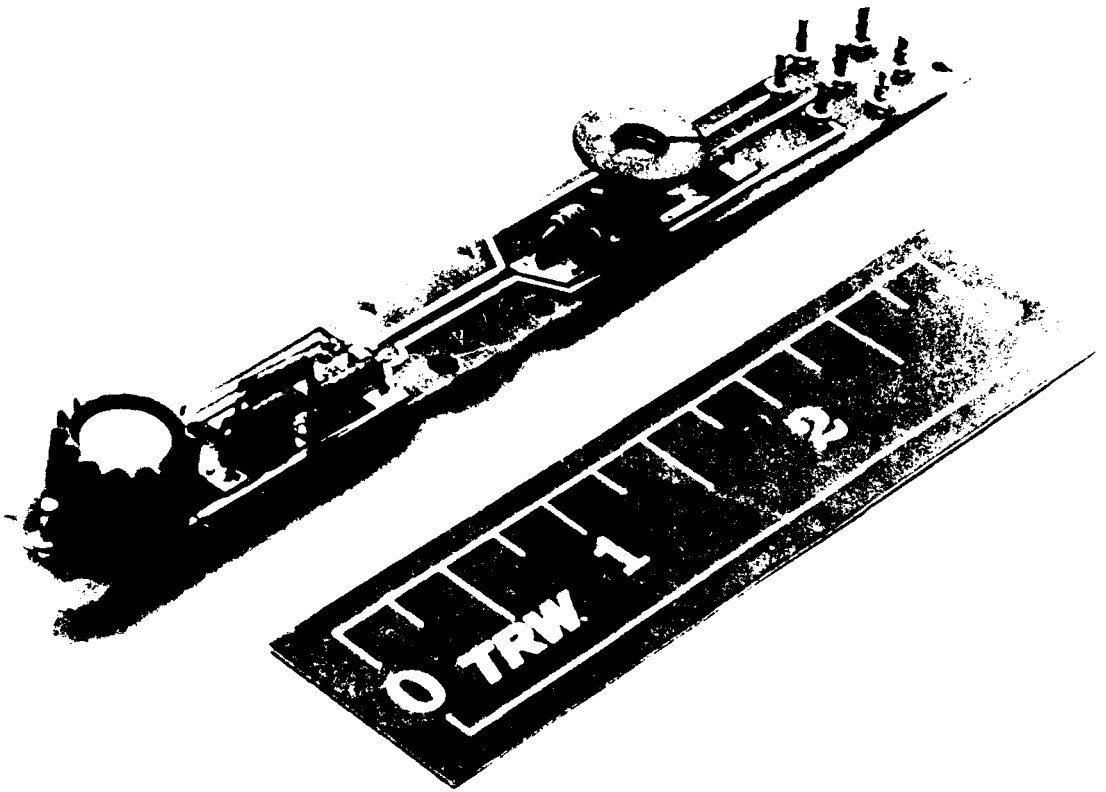


Figure 3-2. DC BOARD CIRCUITRY

3.3 Tone Generation Module

The generation of the reference frequency tones at 486, 526.5, 567 and 607.5 MHz is accomplished through the operation of comb generator circuitry, using a step recovery diode (SRD) design, in conjunction with injection locked oscillator loops employing SAW devices in delay line and bandpass filter configurations. Each of the coherent reference tones are achieved through identical free-running oscillator loops driven in the fundamental mode at a signal power level sufficient enough to achieve a locking bandwidth capability of approximately 150 KHz each. Previous work, supported by ERADCOM, was useful in definition of SAW phase slope properties required for delay line fabrication in this application. Although the injection locking bandwidth of the tone generation module was not specified contractually, a compromise design for the ILO system was chosen for optimized bandwidth-temperature effects considerations. Figure 3-3 shows the general configuration of the tone generation circuitry, and Figures 3-4 and 3-5 show the deliverable tone generator hardware. Figure 3-4 shows the top side of the tone generator slice while Figure 3-5 shows the bottom of the slice with wideband amplifiers and SAW devices mounted so as to allow interconnection to the printed side of the etched duroid board. Note in Figure3-4 that the comb generator circuitry appears in the elongated cavity of the tone generator housing, the remainder of the housing being dedicated to the injection locked oscillators and associated coupler-output filter matching circuitry.

3.3.1 Comb Generator

Generation of line frequencies which are the 12th through 15th multiples of the 40.5 MHz synthesizer input reference frequency is accomplished by utilizing a step recovery diode (SRD) as a harmonic generation device. The comb application of the SRD device is basically similar in technique to that of a CW frequency multiplier, except for the absence of a resonant output network in the comb generator circuit. The comb generator application feeds its output to a wideband resistive network, thereby preserving its output as an impulse train waveform and associated comb spectrum.

The schematic of the comb generator circuitry is shown in Figure 3-6.

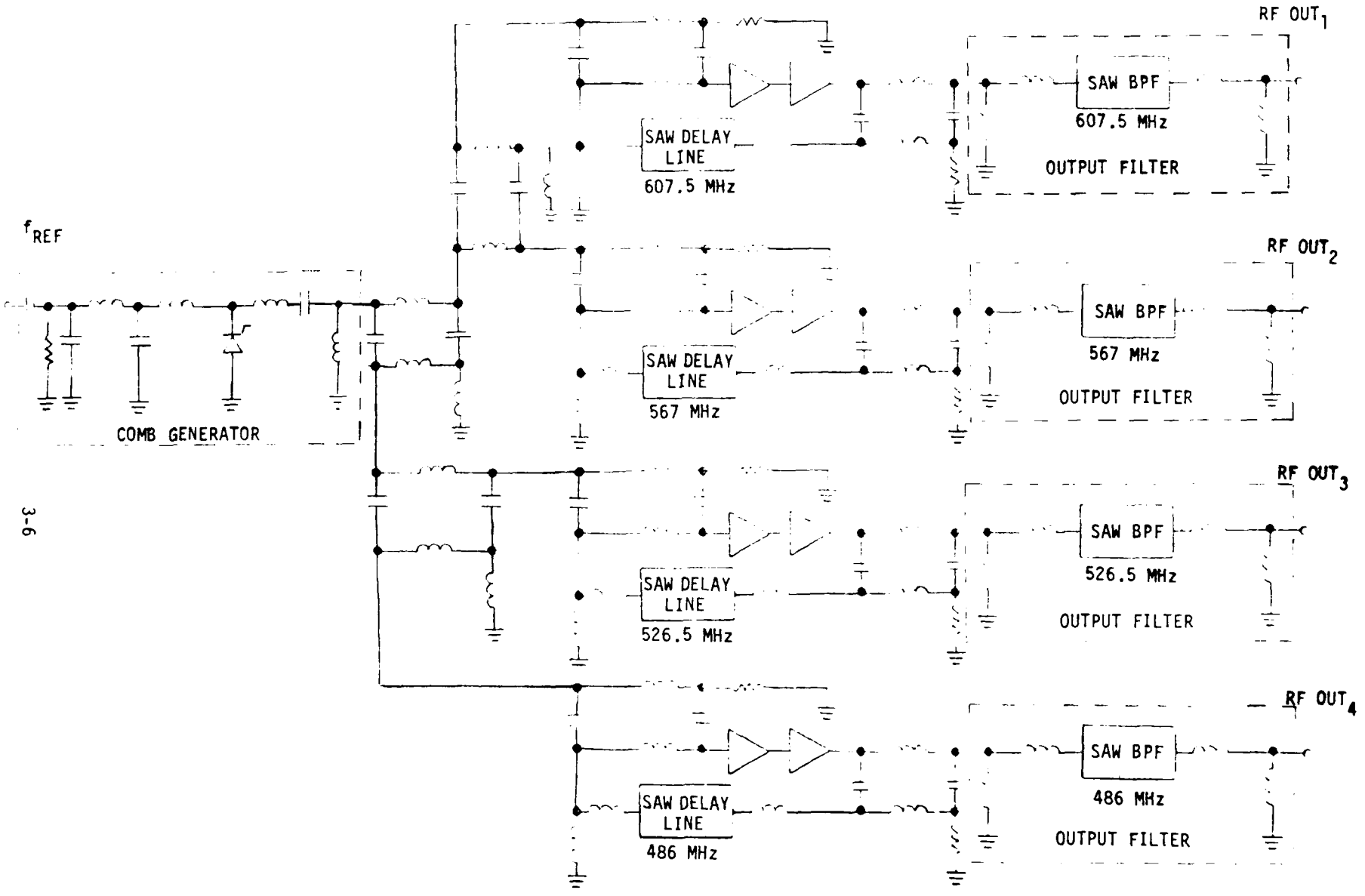


Figure 3-3. TONE GENERATION CIRCUITRY

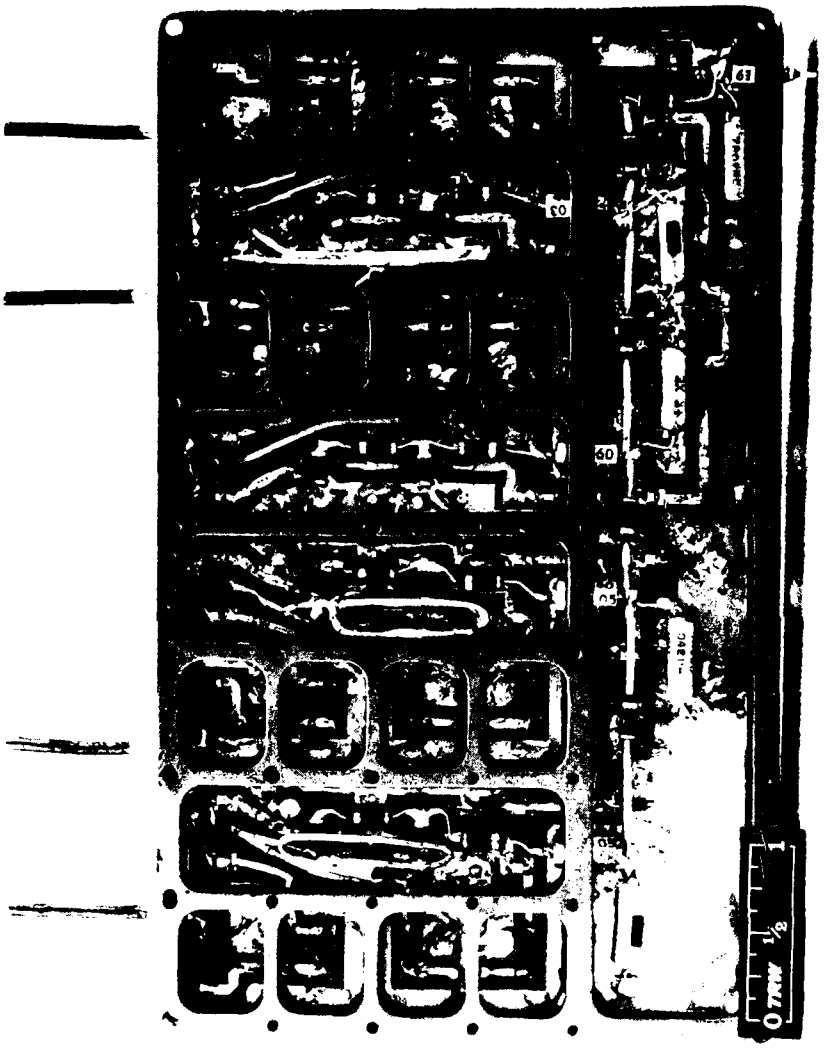


Figure 3-4. TOP VIEW: TONE GENERATION CIRCUITRY

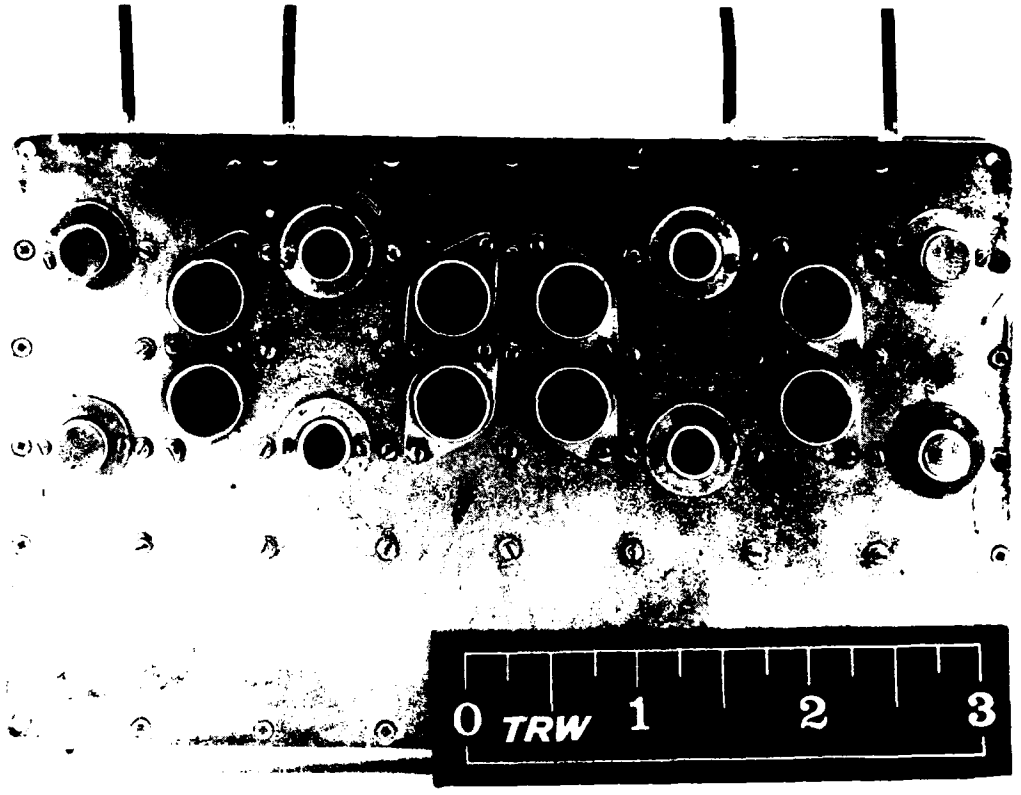


Figure 3-5. BOTTOM VIEW: TONE GENERATOR CIRCUITRY

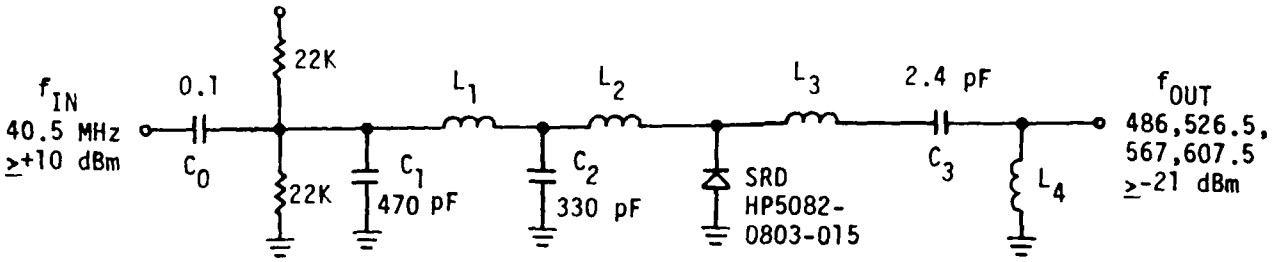


Figure 3-6. COMB GENERATOR SCHEMATIC

The comb generator hardware can be broken down into three principal sections. These sections are: (1) impulse generator circuit; (2) output matching network, and (3) diode bias network. Figure 3-7 is a photograph of the breadboard comb generator circuitry.

3.3.1.1 Impulse Generator Circuit

The circuit components utilized for generation of the impulse train waveform consist of the SRD device, the drive inductor L_2, tuning capacitor C_2, and the matching network components L_1 and C_1. Selection of the appropriate SRD device is governed by considering device parameters such as: breakdown voltage, reverse bias capacitance, transition time, package inductance and capacitance.

For a comb generation application, the driving inductance value is derived from the consideration given to the impulse pulse width, t_p, developed by the SRD circuit. The pulse width, defined by Equation 3-1, is seen to be a function of the reverse bias capacitance C_{VR} of the SRD device and the driving inductance L of the impulse generator circuitry, and is chosen based on where the first zero in the comb line spectrum is to occur (f = 3/2 tp), or on the power variation required between two harmonics of the input frequency, f_{IN}.

$$t_p \simeq \pi\sqrt{LC_{VR}} \qquad (3\text{-}1)$$

The value of the tuning capacitor (C_T) is chosen to resonate with the driving inductance at the input frequency f_i. Its value is given approximately by:

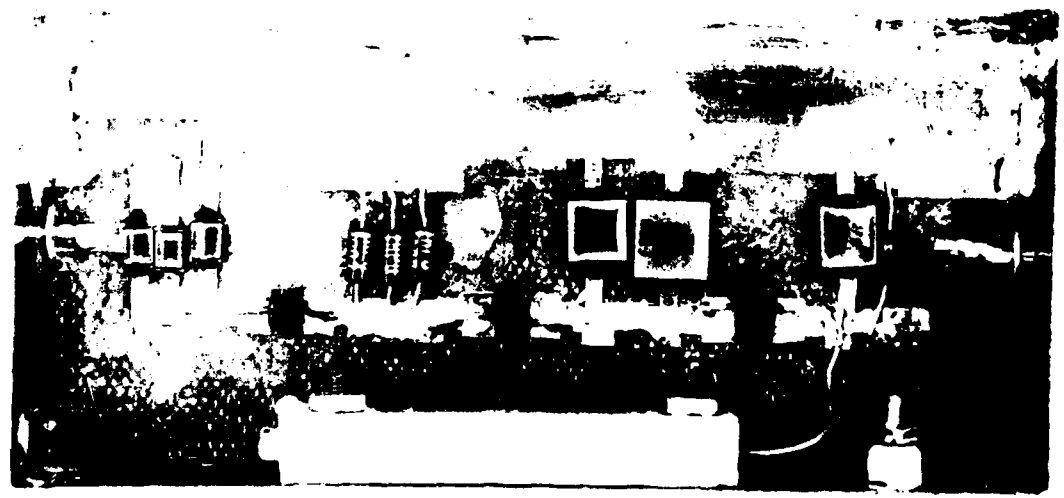


Figure 3-7. BREADBOARD COMB GENERATOR

$$C_T \simeq \frac{C_{VR}}{(2f_{IN}t_p)^2}$$

The matching network components L_M and C_M are designed so as to provide maximum input signal power transfer to the impulse generator circuitry comprised by L, C_T and the SRD device. The impedance seen looking into the shunt C_T is given as R_{IN} by:

$$R_{IN} \simeq \omega_i L$$

where

$$\omega_i = 2\pi f_{IN}$$

For the typical 50 ohm source driving impedance case, where R_g = 50 ohms, and $R_g/R_{IN} \geq 10$, then the element values of the input matching network are given by Equations 3-2 and 3-3 as:

$$L_M = X_M/\omega_i \simeq \frac{\sqrt{R_g/R_{IN}}}{\omega_i} \qquad (3\text{-}2)$$

$$C_M = \frac{1}{X_M\omega_i} \simeq \frac{1}{\sqrt{R_g R_{IN}}\omega_i} \qquad (3\text{-}3)$$

3.3.1.2 Output Matching Network

The circuit components utilized to present a wideband resistive load to the impulse generator circuitry consist of inductor L_3, capacitor C_3, and shunt inductor L_4. The matching network is utilized to translate the reactive load, presented by the multiple twisted-wire couplers of the injection locked oscillator circuitry, to a 50 ohm resistive load required to preserve the comb spectrum of the impulse generator.

3.3.1.3 Diode Bias Network

The bias requirements for the SRD device, although minimal, are supplied by the voltage divider network composed by the 22K ohm resistors as shown in Figure 3-6. While the SRD has a small amount of rectification current flow while in the forward biased state, the magnitude of this current is given by the relationship

$$idc \simeq \frac{2I_p}{\omega_i \tau}$$

where

I_p is defined as the peak current flowing in the drive inductance L just prior to FWD-REV snap of diode,

ω_i is the input radian frequency,

τ is defined as the effective minority carrier lifetime (ns).

Figure 3-8 shows the output spectrum of the comb generator deliverable hardware. Only the principle tones at 486, 526.5, 567 and 607.5 MHz are highlighted. Note that the variations in power level from tone-to-tone is approximately 1.9 dB over the 121.5 MHz band.

3.3.2 Injection Locked Oscillators

Four independent SAW injection locked oscillator circuits with input-output twisted wire 3 dB couplers were designed to provide stable reference frequency generation for the signal processing module. The SAW oscillators provide excellent phase noise and can be designed to be far more temperature stable than conventional microwave oscillators. The primary limitation to many SAW oscillator applications is the temperature stability attainable. Even for SAW devices fabricated on ST-cut quartz, although good, temperature stability is often inadequate to meet desired system requirements. A solution to providing stable frequency generation is to injection lock a bank of SAW oscillators to a comb of frequencies generated from a stable, low noise source. This is the approach that TRW has taken to achieve phase coherency with the 40.5 MHz reference input frequency, while judicious design of the SAW devices incorporated in the oscillator loops has been undertaken to account for the temperature effect related to frequency stability.

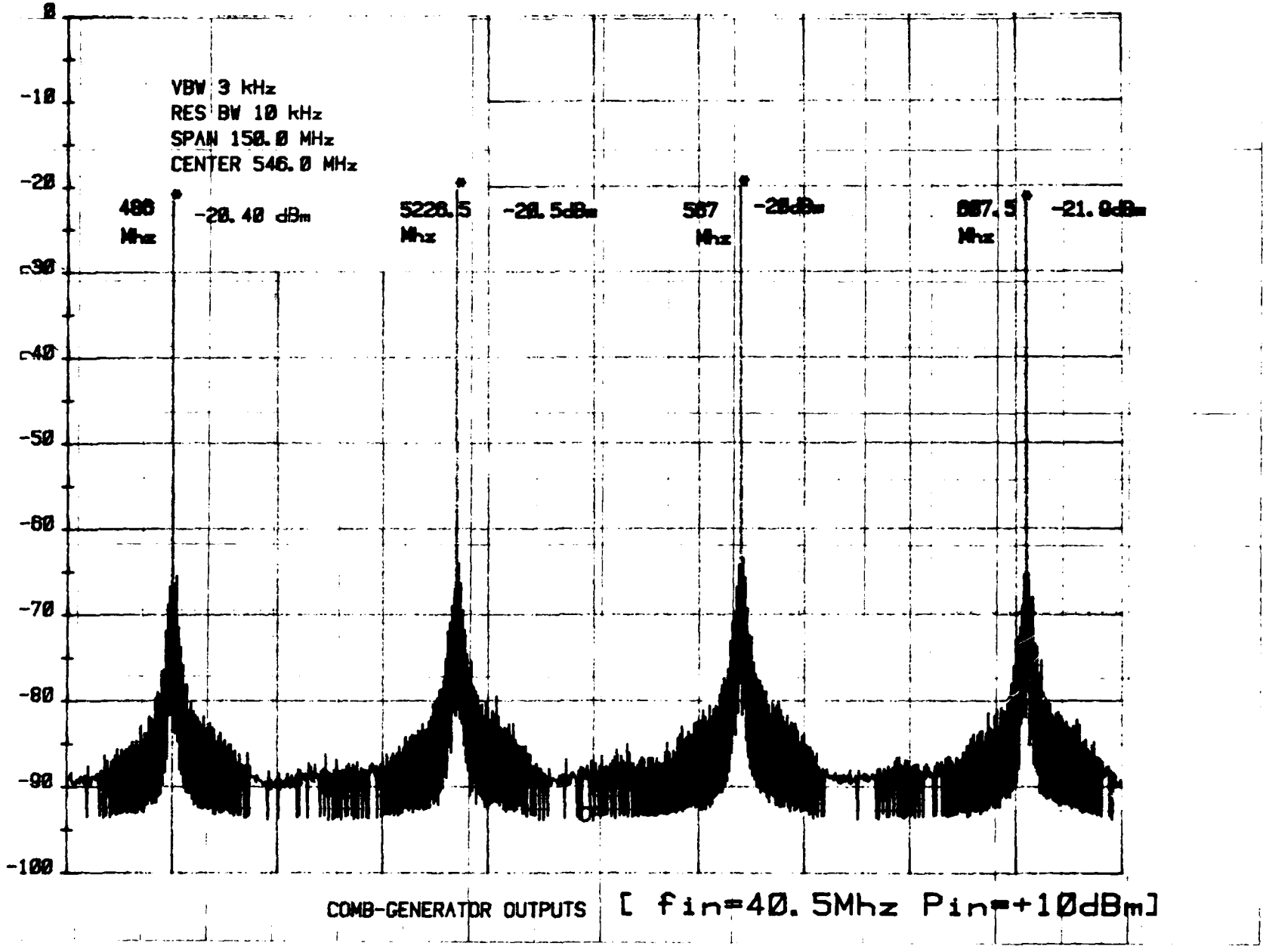


Figure 3-8. COMB GENERATOR OUTPUT SPECTRUM

Figure 3-9 shows a photograph of a single frequency breadboard ILO circuit. Each injection locked oscillator module design incorporates dual wideband RF amplifiers in a feed-forward gain block with a SAW delay line device utilized in the feedback path. The magnitude of the composite amplifier gains is designed to satisfy the condition of oscillation at a frequency within their gain passband defined by the insertion loss characteristics of the delay line. Sufficient loop gain margin is provided to insure stable frequency generation as well as to establish the minimum input drive level required to provide sufficient injection locked bandwidth. Center frequency tunability is achieved by adjustment of loop phase in a lumped delay line section provided in the feedback network.

Two SAW devices are utilized in each of the four oscillator loops. One for achieving loop frequency vs temperature stability and the other for filtering adjacent loop carrier tones, presented in the comb generator output spectrum, which are inadequately filtered by the amount of sidelobe rejection offered by the SAW delay lines. Figure 3-10 shows the schematic representation of a single frequency ILO circuit designed to operate from the comb generator to supply the 486 MHz coherent output. Note the use of the discrete coupler circuitry at the comb generator output and SAW output filter input. These couplers achieve a 3 dB power splitting capability over a wide bandwidth and are attractive for applications where size reduction is a desired feature.

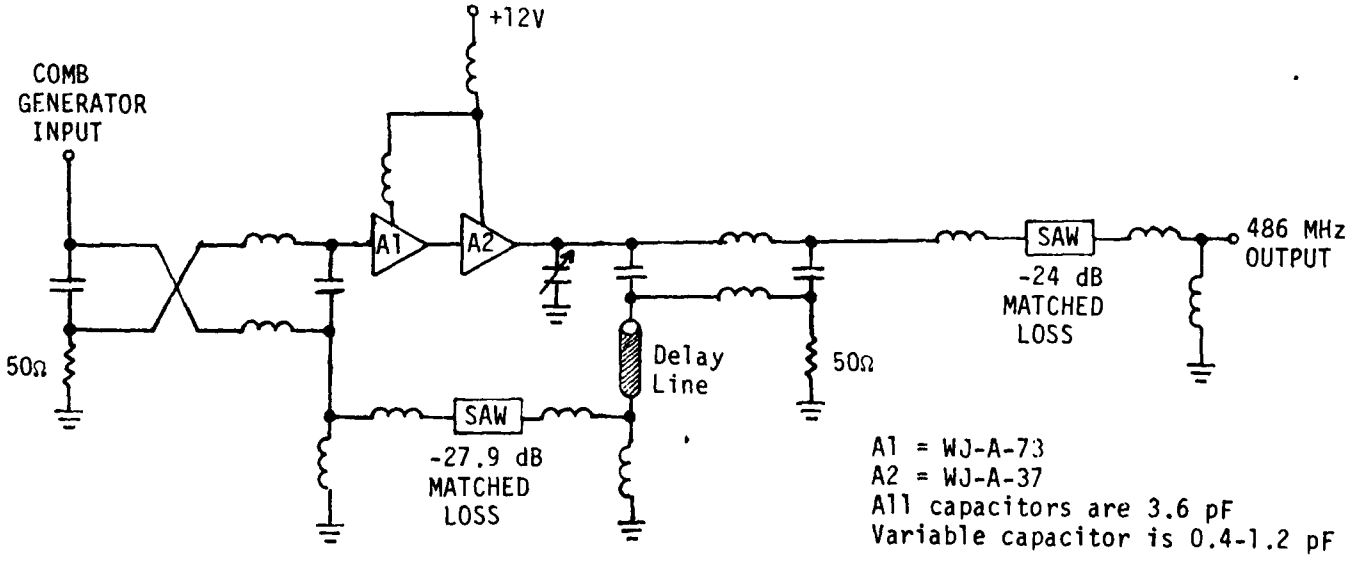


Figure 3-10. 486 MHz ILO CIRCUITRY

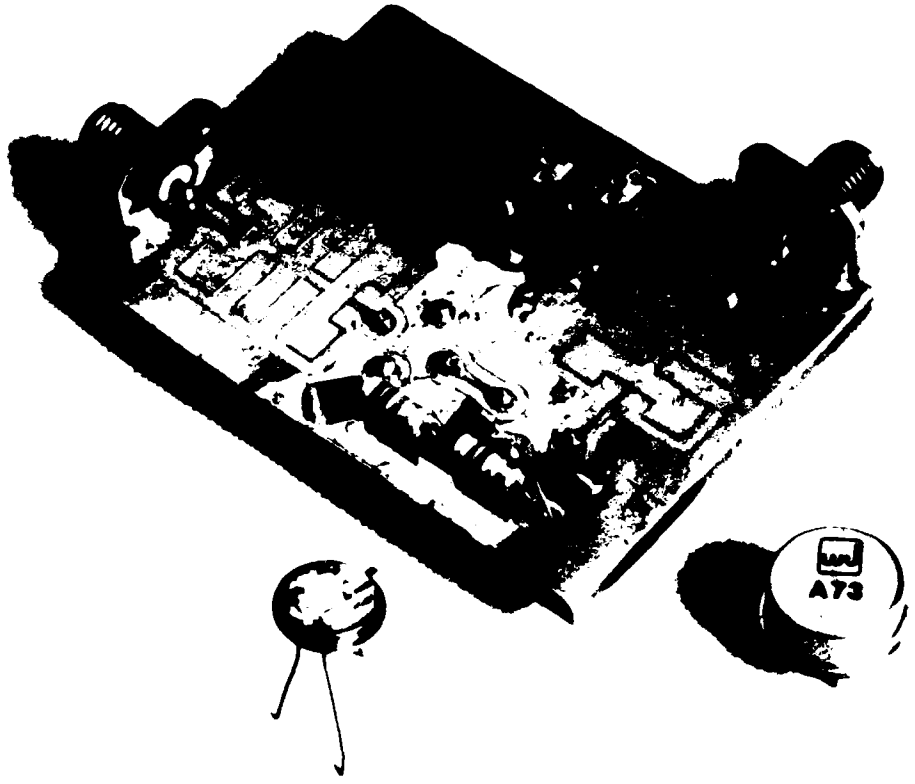


Figure 3-9. BREADBOARD ILO CIRCUITRY (SINGLE FREQUENCY)

Figure 3-11 shows the combined output spectrum of the injection locked oscillators. The spectrum displayed is obtained by applying all four ILO circuit outputs to a 4-way power splitter. The "summed" input port spectrum is viewed on an HP8568A spectrum analyzer via the storage hold mode. Note that with the oscillators locked to the 40.5 MHz reference input, a power level variation of 3.7 dB is obtained over the operating bandwidth.

3.3.3 SAW Delay Lines

The delay lines for the four oscillator circuits were designed to provide a sufficient injection locked bandwidth necessary to overcome the temperature variation drift in oscillator center frequency. Phase variation of the SAW delay line due to temperature change has the effect of producing loop oscillation over a frequency range given (for ST-cut quartz) by

$$\Delta f = f_o(3.2 \times 10^{-8}/°C^2)(\Delta T)^2$$

Over a 70°C operating temperature range with initial oscillation established at 607.5 MHz, the maximum carrier frequency shift expected could achieve 95 KHz. With a ratio of injected signal power to power fed back around the loop of -10 dB, the required SAW device delay to hold lock can be calculated from

$$BW_{INJ} = \frac{1}{\pi\tau}\left(\frac{P_{IN_j}}{P_{f_B}}\right)^{1/2}$$

$$(2 \times 95 \times 10^3 \text{ Hz}) = \frac{1}{\pi\tau}\left(\frac{1}{10}\right)^{1/2} \text{ where it can be shown that}$$

$$\tau \leq 530 \text{ ns}$$

This calculation assumes that the turn-around temperature for the delay line occurs at 15°C ambient temperature, and that coarse adjustment of the loop frequency be achieved at this temperature. The delay line specification, given in Table 3-1, indicates that a fabrication requirement for device delay of 0.25 μs was used to obtain roughly twice the calculated delay. This is due to the desire to obtain injection locked operation over twice the given temperature range about the turnaround temperature.

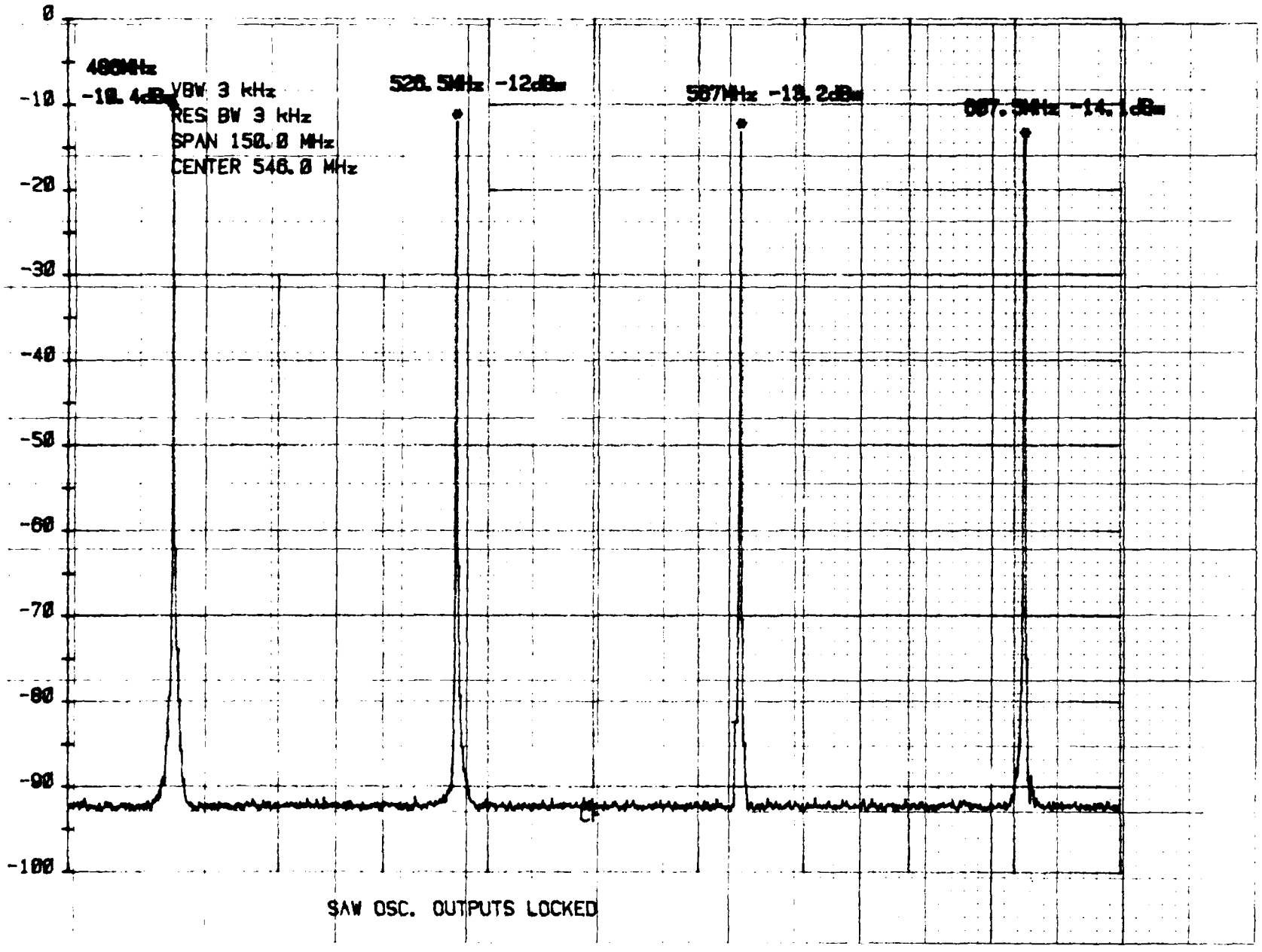


Figure 3-11. LOCKED ILO OUTPUT SPECTRUM

Table 3-1. SAW DELAY LINE SPECIFICATIONS

Center Frequency (MHz)	486, 526.5, 567, 607.5
Insertion Loss (dB)	$\leq$23 (matched)
Time Delay (μs)	$\leq$0.25
Sidelobe Rejection	30 dB min. at 40.5 MHz from f_o
Turnover Temperature	15°C $\pm$5°C

Table 3-2 indicates the design parameters pertinent to fabrication of the delay line devices.

Table 3-2. SAW DESIGN PARAMETERS

Center Frequency (MHz)	No. of Pairs Per Transducer	Acoustic Aperture (λ_o)*	Finger Width (μm)	Center-to-Center Separation Between Transducers (λ_o)	Al Metallization Thickness (Å)
486.0	32	90	2.43	105	750
526.5	32	90	2.24	105	700
567.0	32	90	2.08	105	650
607.5	32	90	1.94	105	600

* λ_o = Acoustic wavelength at the center frequency.

In the microwave oscillator SAW delay line design, each delay line consists of two identical transducers with split electrode configuration. The transducers operate at the third harmonic and the finger width stays well within the resolution limit of conventional photolithographic techniques. Figure 3-12 shows the fabricated delay line device prior to packaging.

Figure 3-12. SAW DELAY LINE DEVICE

The substrate chosen for these delay lines is CT-cut quartz with $\theta = 38°$. The reason for using the CT-cut instead of the ST is due to the fact that nearly half of the substrate surface in the SAW delay line region is covered with aluminum metallization. This metallization lowers the turnover temperature or the temperature at which the SAW center frequency exhibits minimum frequency change. With the presence of this metallization, the most temperature stable cut is not longer ST-cut but is CT-cut, when the proper metallization thickness is employed. Figure 3-13 shows the delay line packaged in a TO-5 carrier, utilized for this application to minimize the size required by the overall tone generator module circuitry.

3.4 Synthesizer Module

The hardware incorporated in the synthesizer module comprises both discrete device designs and RF-LSI circuitry to provide for generation of the desired output at one-half the desired output frequency. The technologies utilized to perform the signal switching as well as redundant mix-and-divide functions were obtained via RF-LSI devices, the SP3T and ADM-1 circuitry, respectively. Both the SP3T switch and ADM-1 circuitry are described in detail, with particular detail given to the ADM-1 conglomerate RF-LSI devices.

3.4.1 RF-LSI Circuitry

Processing of the RF signals in the synthesizer module is accomplished via direct synthesis methods. The four primary tones filtered by the band-pass responses of the SAW filters at the ILO outputs are passed onto a multi-layer RF printed circuit board. The 486 MHz output from the tone generator module is routed directly to the LO input of the #1 ADM of the synthesizer module, unlike the other three primary tones. From a common launching point, unique to its own layer in the stack of alternate RF and ground planes, each of the remaining three RF tones are split four ways and presented to the appropriate input ports of the four RF switches. The 486 MHz input of the switches is grounded, as it is not utilized in a selectable input mode, thereby modifying the switches to perform a SP3T function. Each SP3T switch in turn selects the commanded input tone, by means of a two-bit TTL command, amplifies it in level, and applies it to

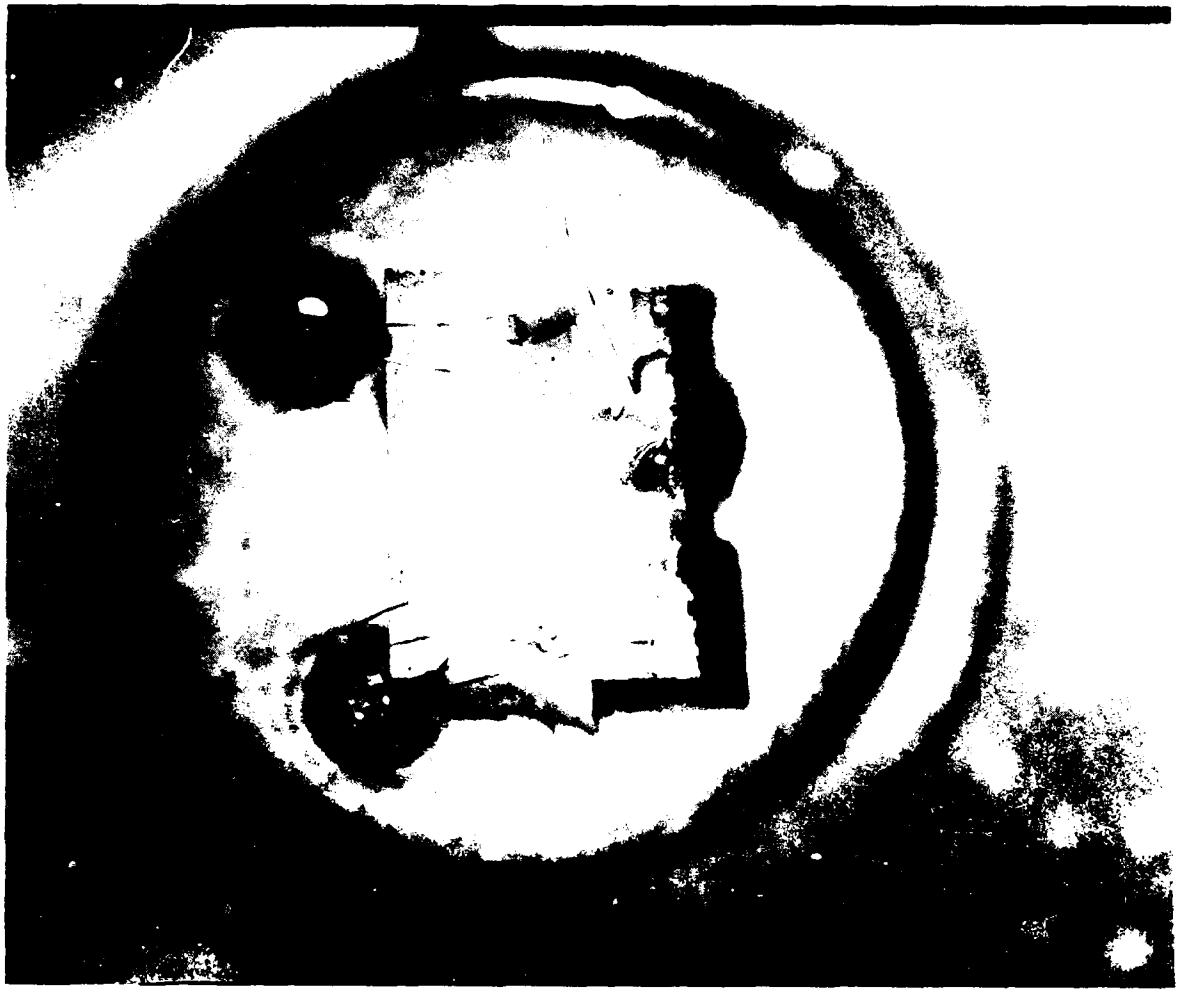


Figure 3-13. SAW DELAY LINE PACKAGED CONFIGURATION

the RF port of the mixer in a programmable mix-and-divide network, ADM-1. The processed IF output of the first ADM-1 is passed from its mixer through a commercial bandpass filter and is applied as the LO input to the second ADM-1's input amplifier. This processing scheme cascades through three successive ADM-1 circuits, thereby producing an output IF spectrum capable of being swept from 648.0 to 768.0 MHz in 1.5 MHz increments.

3.4.1.1 SP3T Switch

The SP3T switch was originally designed to provide 70 dB of isolation of the unselected inputs relative to the selected input, as measured at the switch output. A number of design features were incorporated into the switch circuitry to specifically address this problem. To avoid coupling through power supply or ground impedances, all circuitry is differential. The input signal, as supplied from the multilayer RF board, is single-ended, so the complementary side of each differential input as well as output is brought off-chip and grounded through a bypass capacitor inside the 60-pin package. Also, the selected channel was designed to have gain, so that less attenuation would be required in the unselected input channels.

Some modifications to original design concepts incorporated in the final SP3T hardware were made to enhance noise margin and increase the switch amplifier bandwidth. Stray coupling of unselected channel inputs was reduced in the switch output section by providing separate power supply connections, for each input switch and output, external to the package. In this manner, stray coupling is reduced since signal currents in power supply lines do not have common bond wires and package lead impedances.

Power supplies are +5 volts for VCC and -5 volts for VEE. The select inputs accept TTL levels between 0 and +5 volts. A block diagram for the switch chip layout is shown in Figure 3-14. Note that the layout pays particular attention to equalized line segments from the switch inputs to output section, as well as employs a full differential signal path. These measures are incorporated to minimize switch gain variation at each of the signal frequencies as well as to maximize input-output isolation as mentioned above. Figure 3-15 shows a typical input switch channel to output section signal path in schematic form.

When the switch channel shown in Figure 3-15 is selected, the select input is pulled low, allowing the current sources for the differential pairs to be turned on. In the on state, the selected signal is amplified through two differential common-emitter/common-base cascade stages. The first stage includes diode peaking to flatten the overall frequency response. The gain is stabilized by emitter degeneration resistors and is about 20 dB overall in the selected channel. The second common-base stage serves also to combine the four channels. In the off state, the isolation from input to output is primarily obtained from the two common-base stages, which have provision to reverse-bias their emitter-base junctions when they are not selected.

Extensive computer simulations, using SPICE 2, were performed to investigate frequency performance and temperature stability of the switch. The circuit was simualted in two sections: (1) digital select circuitry; and (2) RF switch amplifier. A transient analysis was used for the digital circuitry, and an AC analysis was performed on the switch amplifier. The computer predicted performance is summarized below in Table 3-3.

Table 3-3. COMPUTER-PREDICTED PERFORMANCE OF CIRCUIT

Switch Amplifier Voltage Gain	17 dB
Temperature Variation of Gain (-55°C to 125°C)	$\pm$1 dB
3 dB Bandwidth	600 MHz
Temperature Variation of Bandwidth (-55°C to 125°C)	$\pm$50 MHz
Switch Amplifier ON/OFF Ratio	>70 dB
Digital Select Circuitry Propagation Delay	10 ns
Temperature Variation of Propagation (-55°C to 125°C)	$\pm$2 ns

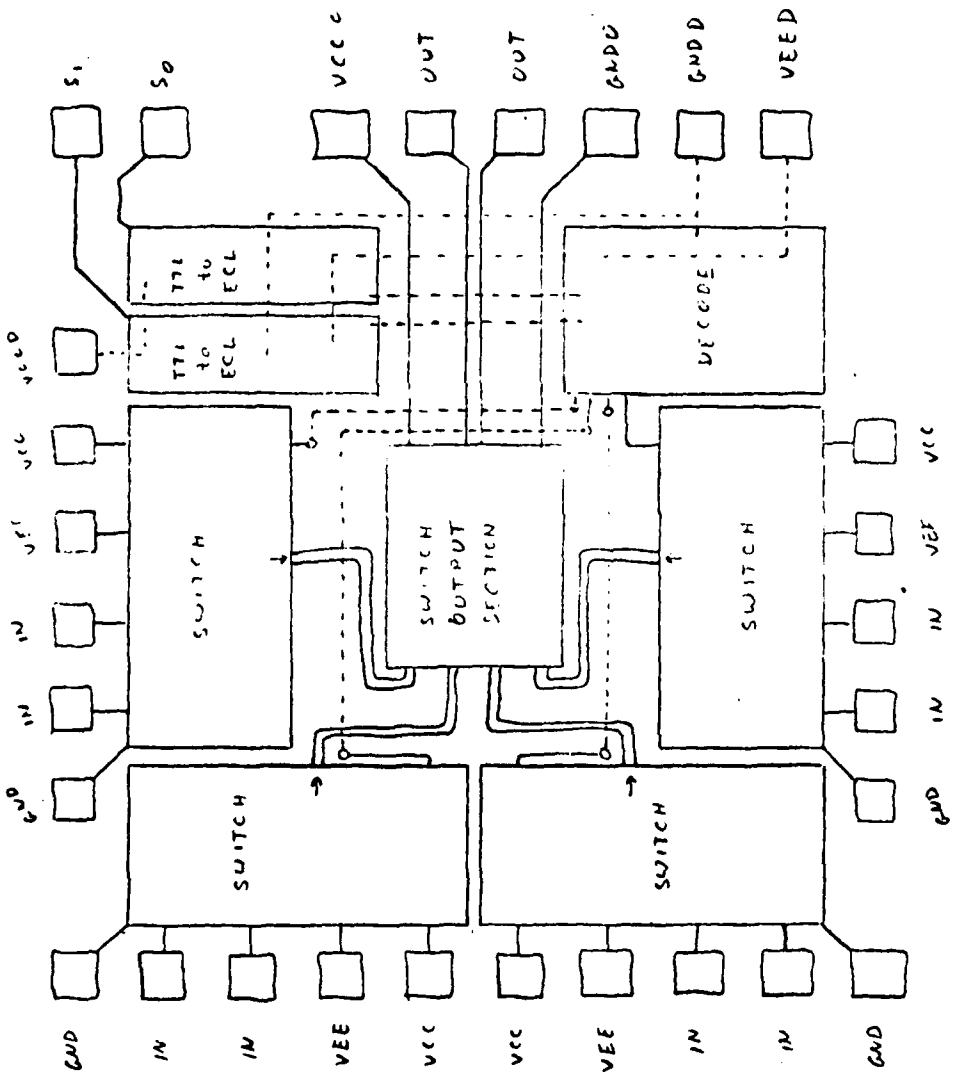


Figure 3-14. SP3T SWITCH PRELIMINARY BLOCK LAYOUT

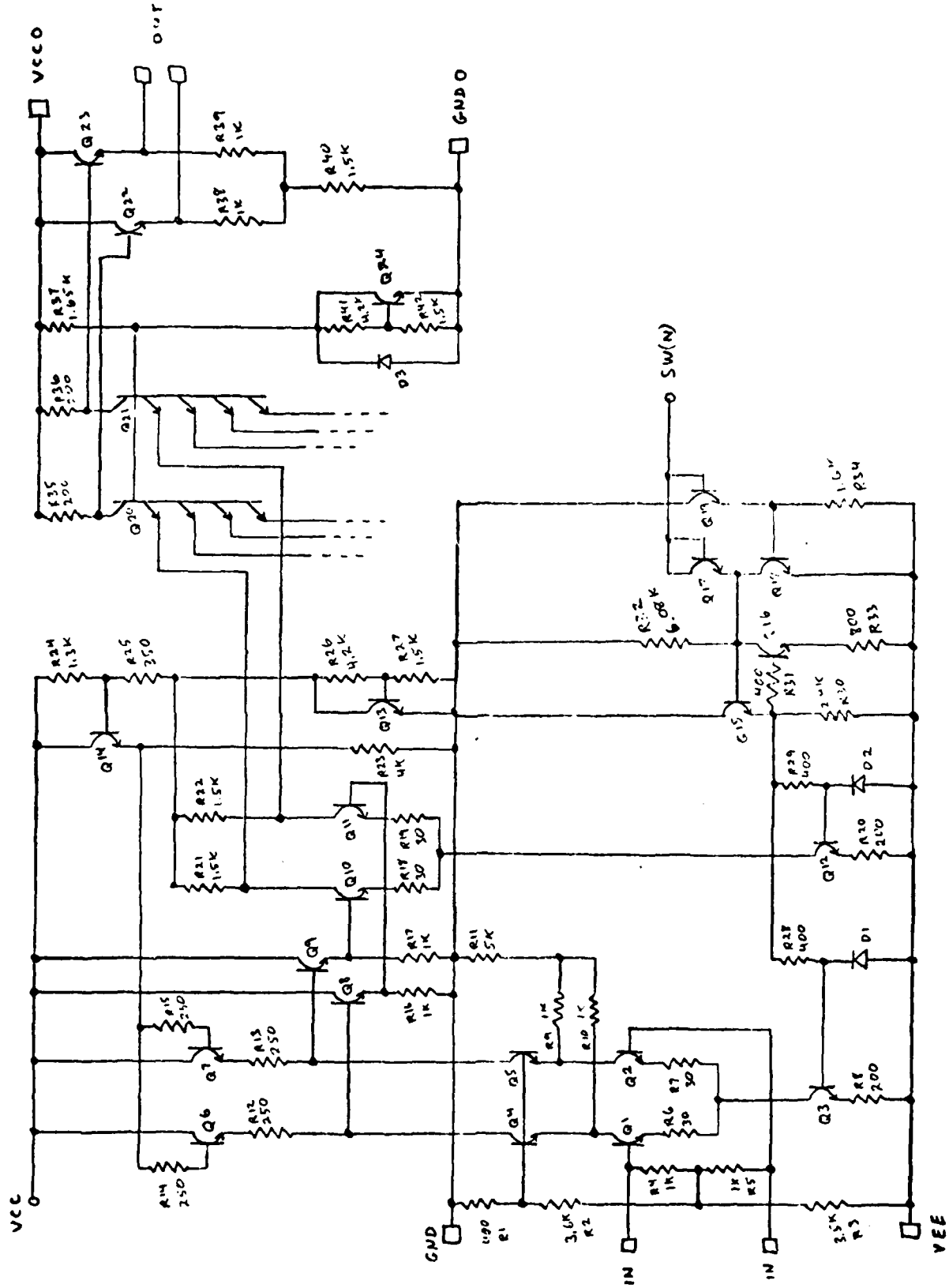


Figure 3-15. SAW SYNTHESIZER: SWITCH; ONE OF FOUR INPUT SECTIONS, COMMON OUTPUT SECTION

Figure 3-16 below shows a photograph of the SP3T switch die, and Figure 3-17 shows the die bonded into a 40-pin flat-pack package.

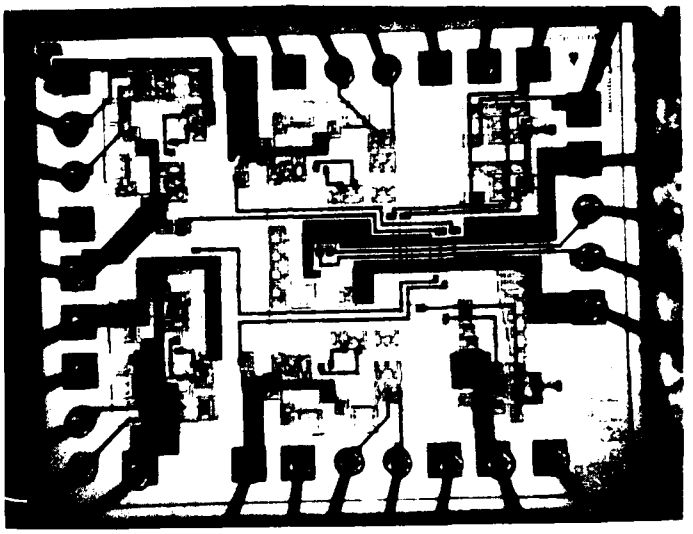


Figure 3-16. SP3T SWITCH DIE PHOTOGRAPH

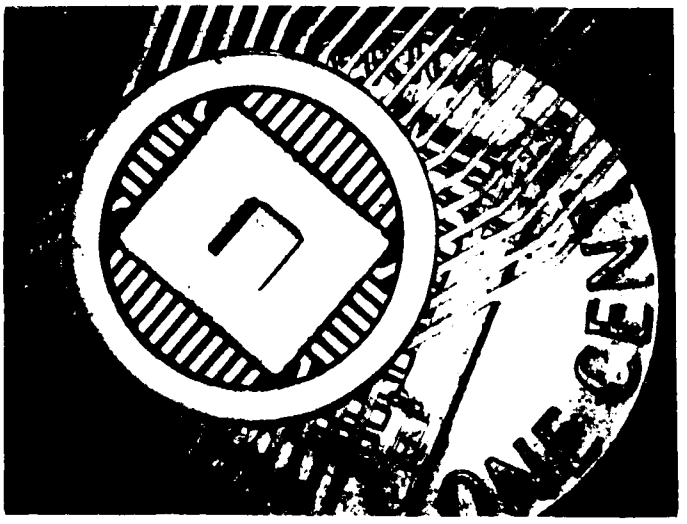


Figure 3-17. SP3T IN 40-PIN PACKAGE

Some comments on the interpretation of computer simulation are in order. A very pessimistic model for the OAT (Oxide Aligned Transistor) device was used in all simulations, therefore it is expected that the computer predictions will be an accurate representation of worst case performance. The gain of the switch amplifier in the OFF state was predicted to be well below -100 dB. This result does not include substrate coupling, or coupling effects associated with the packaging scheme adopted.

Switch isolation was measured for the packaged chip configuration shown in Figure 3-17 and was measured to be only 40 to 45 dB, far below the 70 dB desired. Isolation for the RF test fixture, the packaged switch, and an empty switch package have all been measured. The switch package has been found to be inadequate for this application - providing only approximately 40 dB isolation. A new packaging concept has been investigated. Based on these investigations the chip is being mounted in a CPW (coplanar waveguide) structure. This packaging concept will produce approximately 60 dB RF isolation and will require little more volume than the current approach.

CPW is an ideal medium for launching onto differential RF-LSI circuitry. This transmission medium provides both a signal path and ground path at the chip interface and thereby enhances a common mode rejection. Figure 3-18 shows a sketch of a CPW, basically a narrow strip with two ground planes

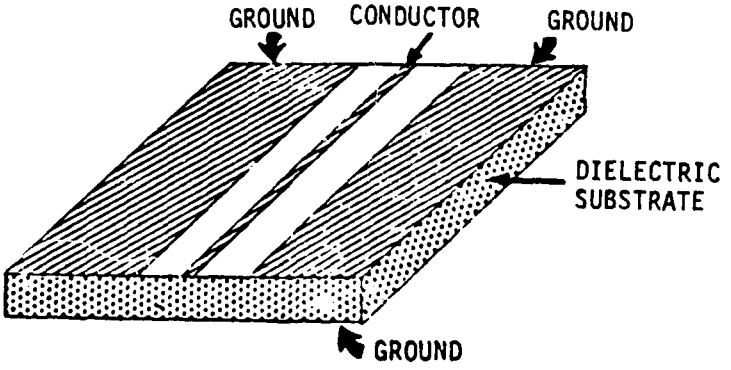


Figure 3-18. COPLANAR WAVEGUIDE WITH GROUND PLANE

running adjacent and parallel to the strip on the same side of a substrate. Classically, CPWs are characterized by their characteristic impedance and phase velocity calculated by assuming that the dielectric substrate is thick enough to be considered infinite.[1] However, in the current application, a ground plane is used not only adjacent to the conductor but on the other side of the relatively thin dielectric substrate. The analysis to calculate this perturbation has been developed at TRW[2] and is based on a finite difference method with a network elimination technique. Figure 3-19 shows the change in characteristic impedance for the particular geometry described in the figure as the ground plane (L_1) distance is moved closer to the dielectric. Very good agreement has been obtained between measurement and the calculations.

Figure 3-20 below shows the SP3T switch mounted in a 60-pin package with the coplanar waveguide substrate.

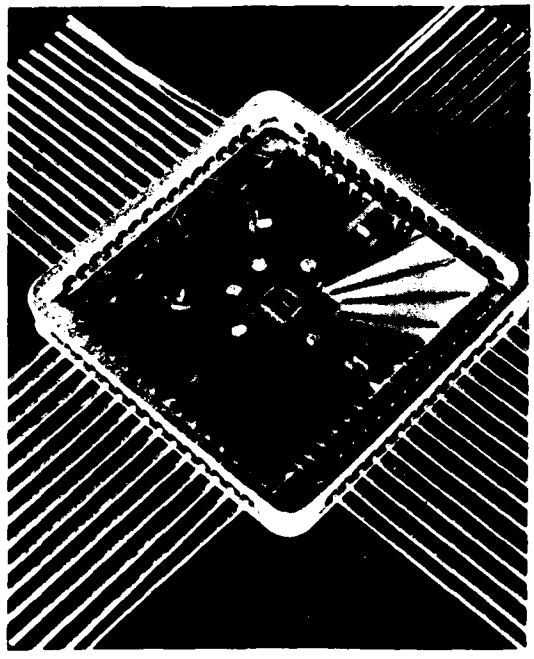


Figure 3-20. SP3T SWITCH

[1] C.P. Wen, "Coplanar Waveguide: A Surface Strip Transmission Line Suitable for Nonreciprocal Gyromagnetic Device Applications", Vol. MTT-17, pp. 1087-1090, December, 1969.

[2] C.L. Chao, "Computation of Coplanar Waveguides", TRW IOC 76-7327-S-14, June, 1976.

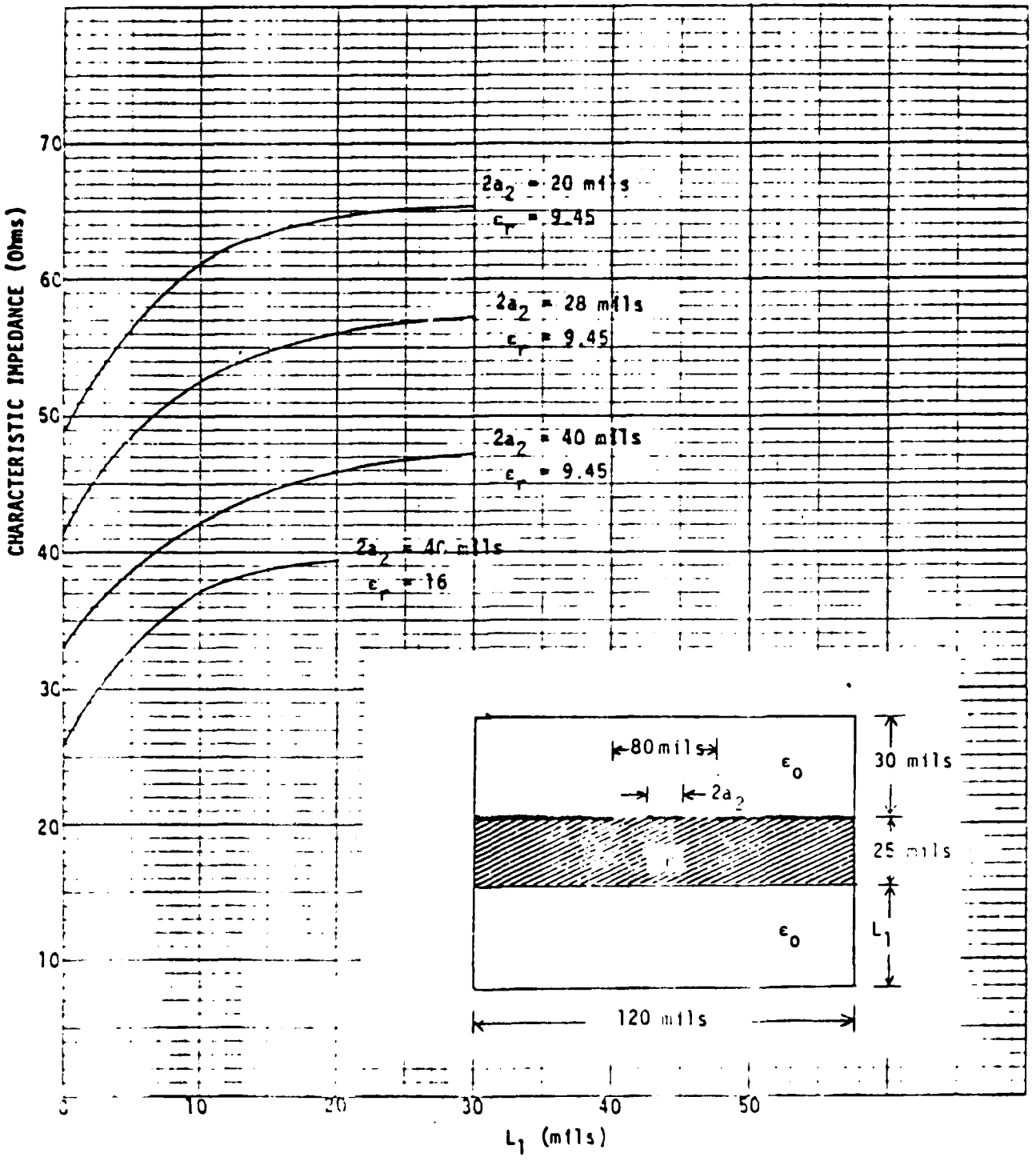


Figure 3-19. IMPEDANCE vs GROUND PLANE PROXIMITY FOR COPLANAR WAVEGUIDE

The switch was characterized in this new configuration, with unmatched inputs and output. A brief summary of its performance is given in Table 3-4 below. Figures 3-21 through 3-24 show typical measured selected channel gain as well as unselected channel isolation as measured at the switch output.

Table 3-4. TYPICAL SP3T PERFORMANCE

Selected Channel Voltage Gain (Unmatched)	10 dB
Unselected Channel Isolation	50-60 dB
Switching Speed	$\leq$15 ns
Power Consumption	$\leq$0.28 W

Figure 3-25 shows SP3T switching speed as well as the test conditions under which the measurement was made. Switching speed for both turn-on and turn-off is approximately 10 ns, well within the synthesizer requirement of $\leq$1 µs.

Figures 3-26 and 3-27 are measurements made on the unmatched switch at all input and output ports. The magnitude of the input and output reflection coefficients is approximately 0.88, which represents input and output mismatch losses of 13 dB.

Figures 3-28 through 3-32 are the detailed switch block diagram as well as individual switch chip module schematics.

3.4.1.2 ADM-1 (Mix-and-Divide Circuitry)

The central signal processing hardware of the direct synthesis design is the RF-LSI circuitry designed to perform the redundant mix-and-divide functions, or ADM-1, abbreviated for Amplify-Divide-Mix.

The complete task of amplifying, dividing (programmable as ÷3 or ÷4), filtering, and mixing the LO signal with the selected RF signal from the SP3T switch was to be accomplished by a single RF-LSI chip. More specifically, the ADM-1 circuitry was designed as a monolithic IC utilizing conventional RF design techniques incorporated in front end and output amplifiers, a five-latch design using standard low-level differential logic circuits in the divider, an emitter-follower/diode level shifter with diode peaked differential lowpass filter, and a variable transconductance four-quadrant-multiplier mixer stage with differential output buffering circuitry to present a 50 ohm output impedance to off-chip bandpass filters.

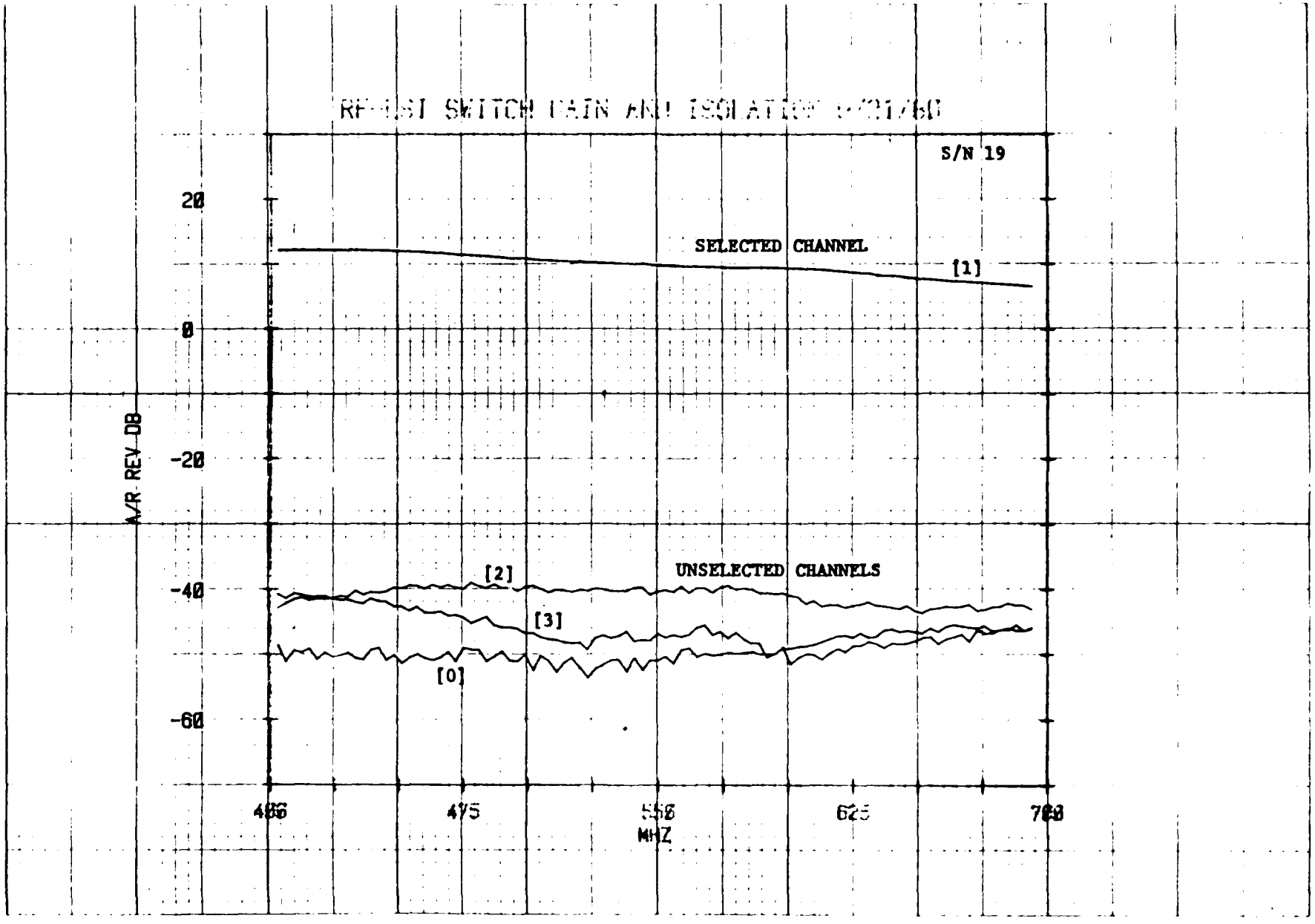


Figure 3-21. RF-LSI SWITCH GAIN AND ISOLATION

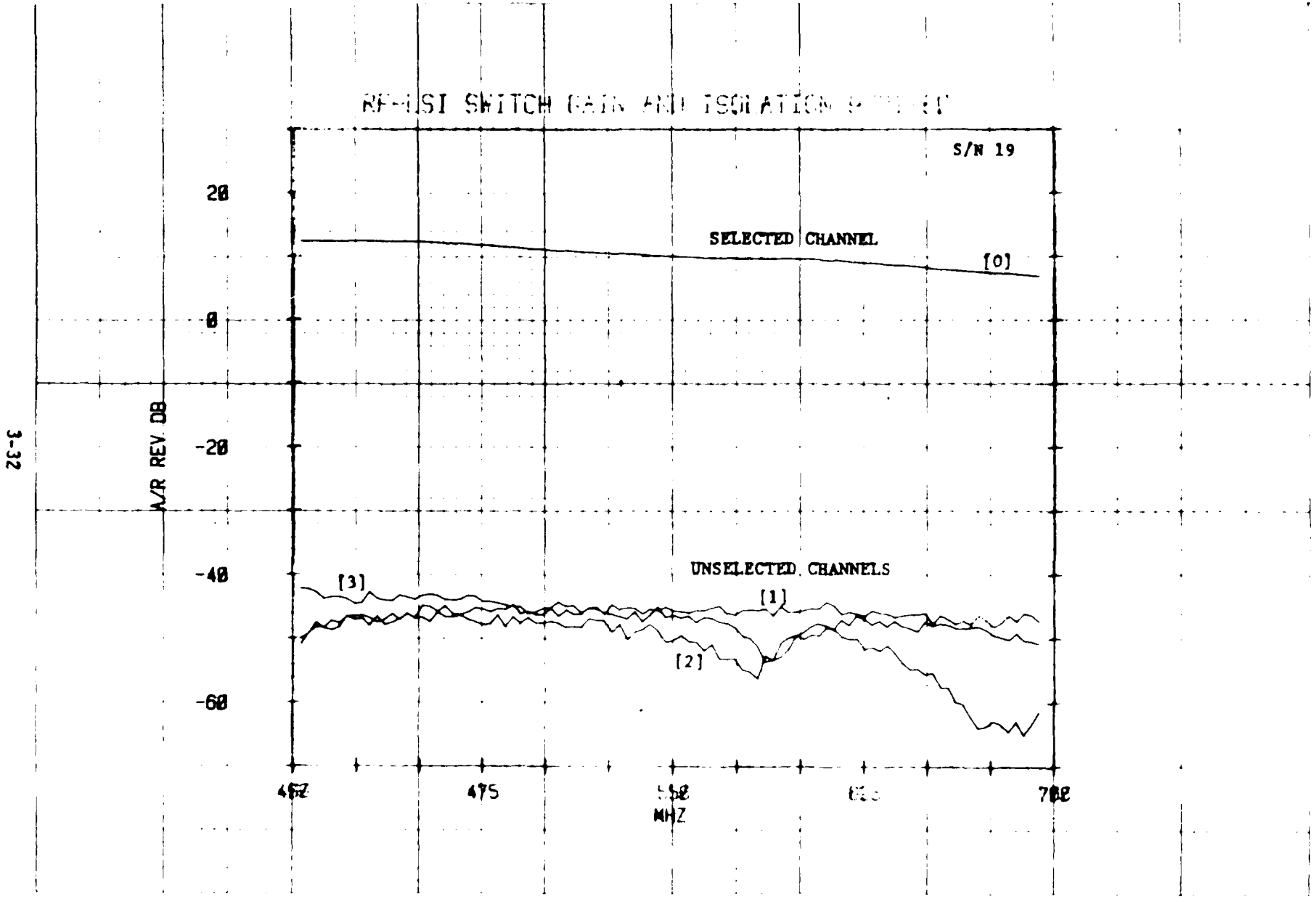


Figure 3-22. RF-LSI SWITCH GAIN AND ISOLATION

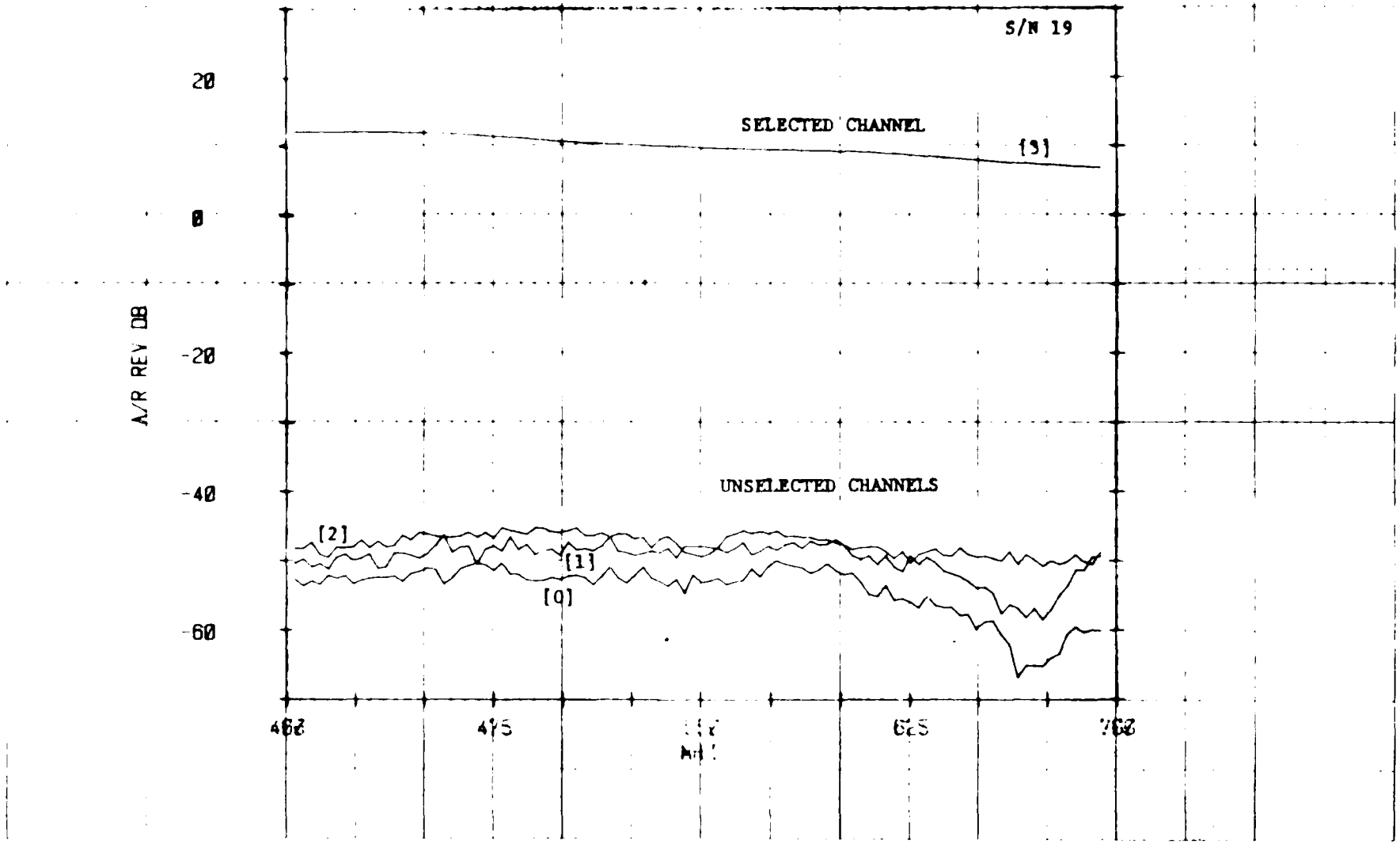


Figure 3-23. RF-LSI SWITCH GAIN AND ISOLATION

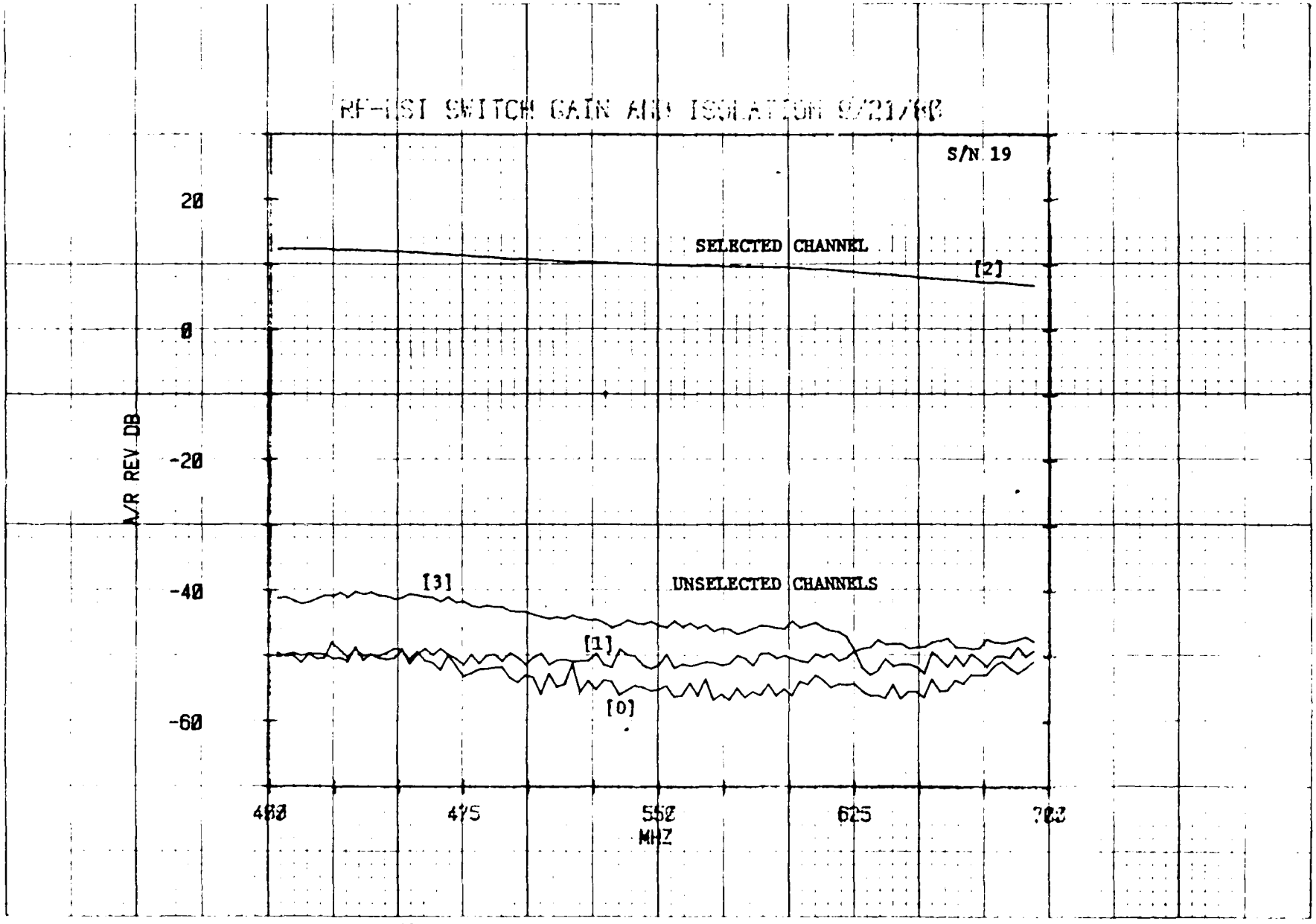
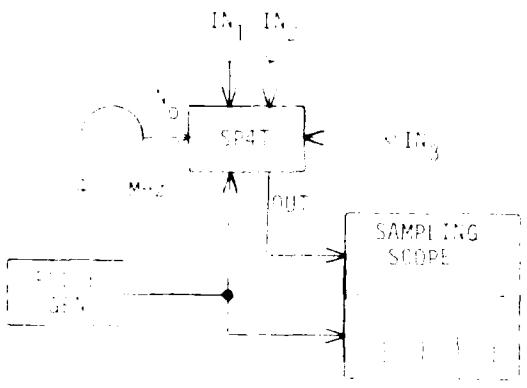
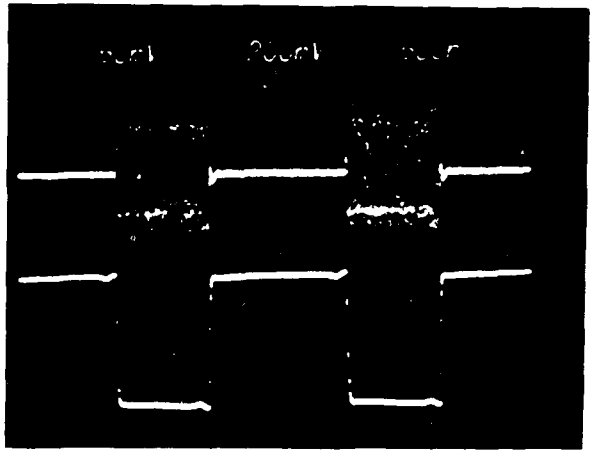
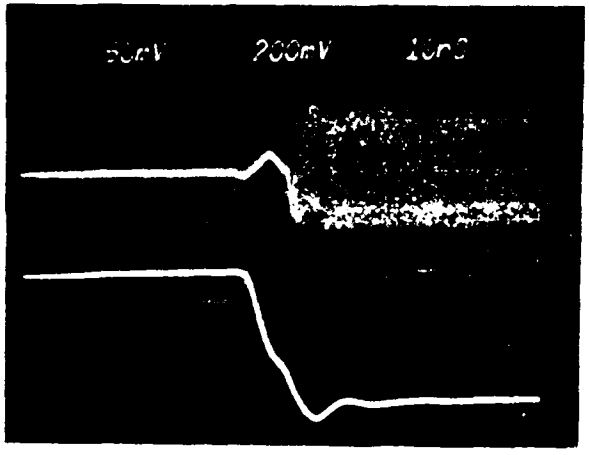
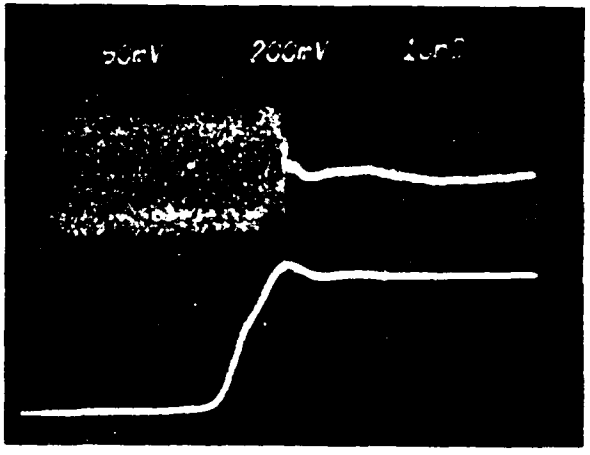


Figure 3-24. RF-LSI SWITCH GAIN AND ISOLATION









RF-LSI SP3T SWITCH, SWITCHING SPEED

NAME	TITLE REFLECTION COEFFICIENT, CHANNEL 1,2,3	DWG NO
SMITH CHART FORM 82-65DR (9-66)	KAY ELECTRIC COMPANY PINE BROOK N J © 1966 PRINTED IN U.S.A.	DATE

IMPEDANCE OR ADMITTANCE COORDINATES

Freq.=300-1300 Mhz.

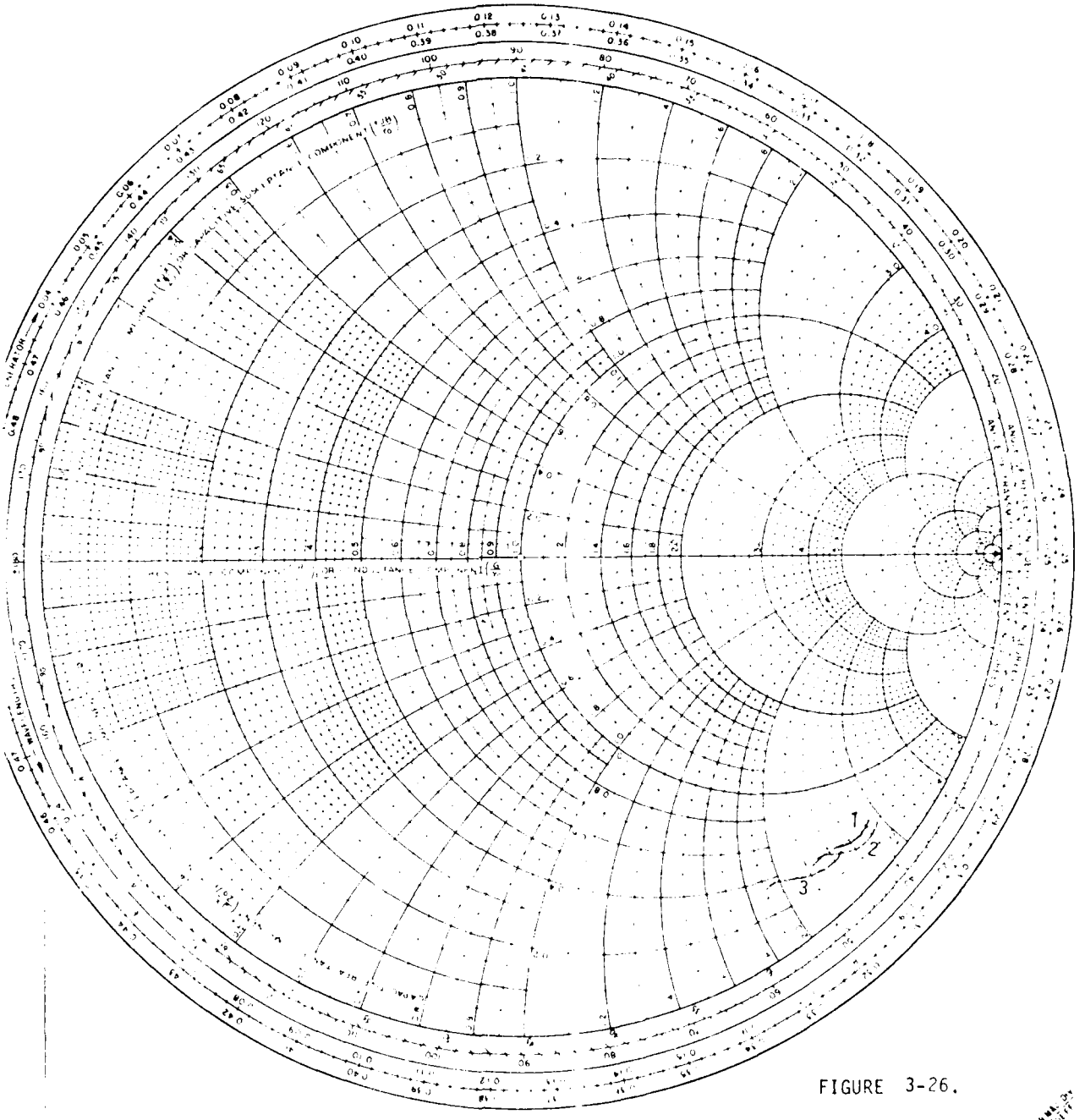
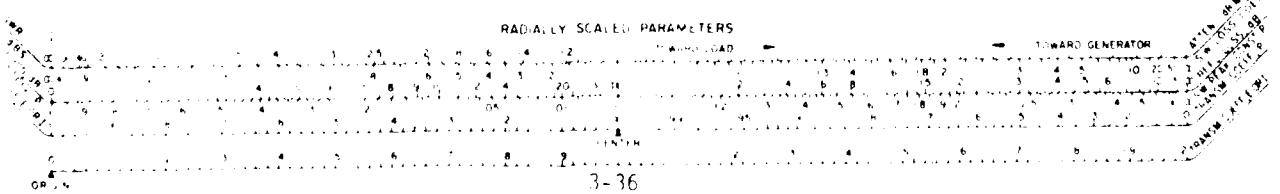


FIGURE 3-26.



NAME	TITLE	DWG NO
SMITH CHART FORM P-(9-66)	REFLECTION COEFFICIENT, CHANNEL 0 AND OUTPUT	
	KAY ELECTRIC COMPANY PINE BROOK N J © 1966 PRINTED IN U.S.A.	DATE

IMPEDANCE OR ADMITTANCE COORDINATES Freq.=300 1300 Mhz.

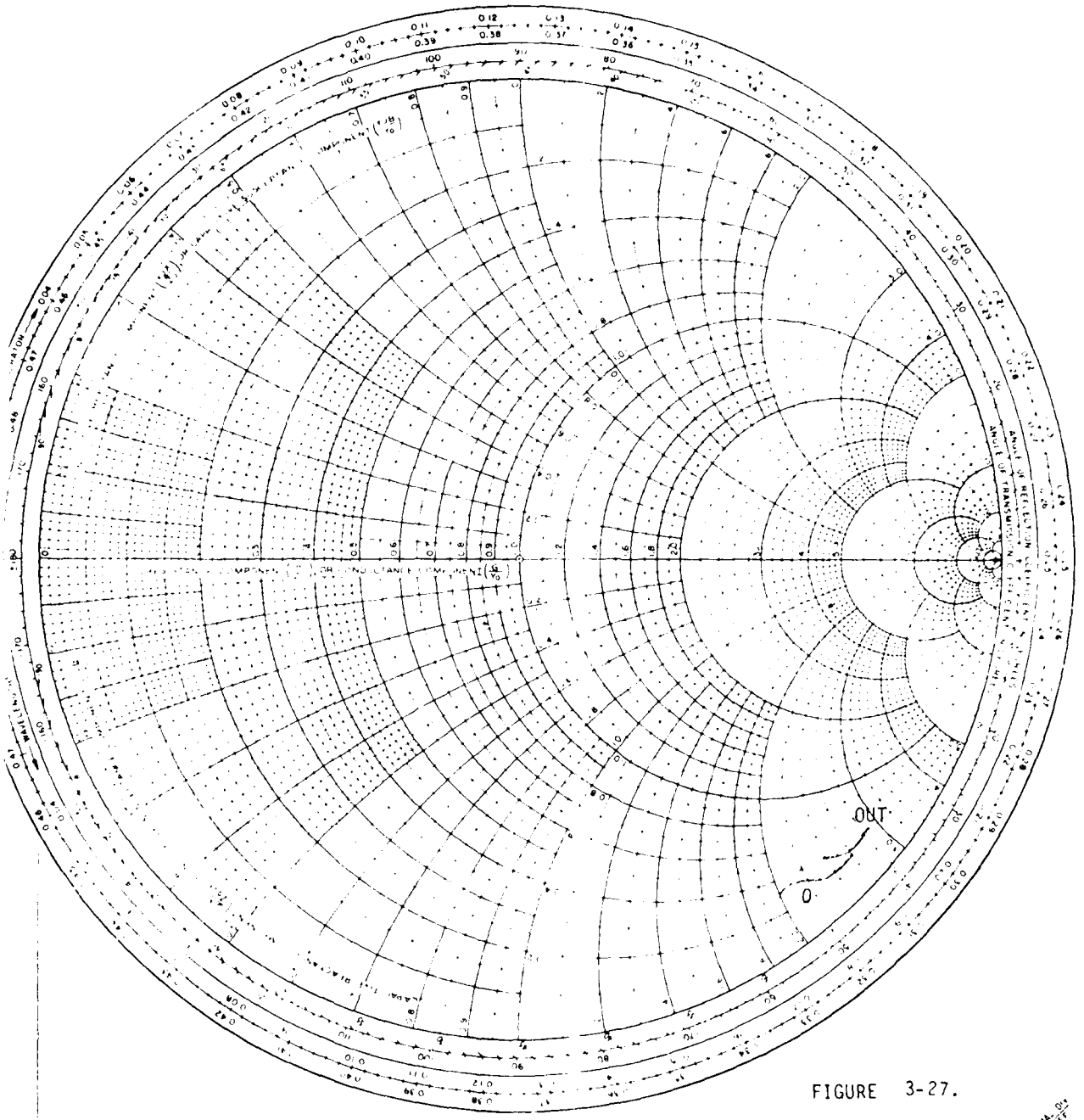
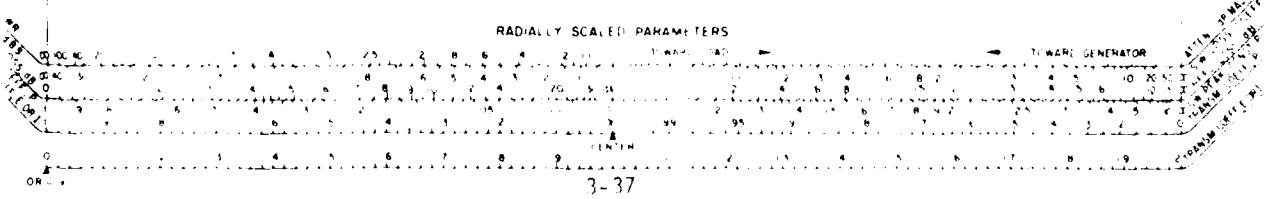


FIGURE 3-27.



A MEGA-CHART

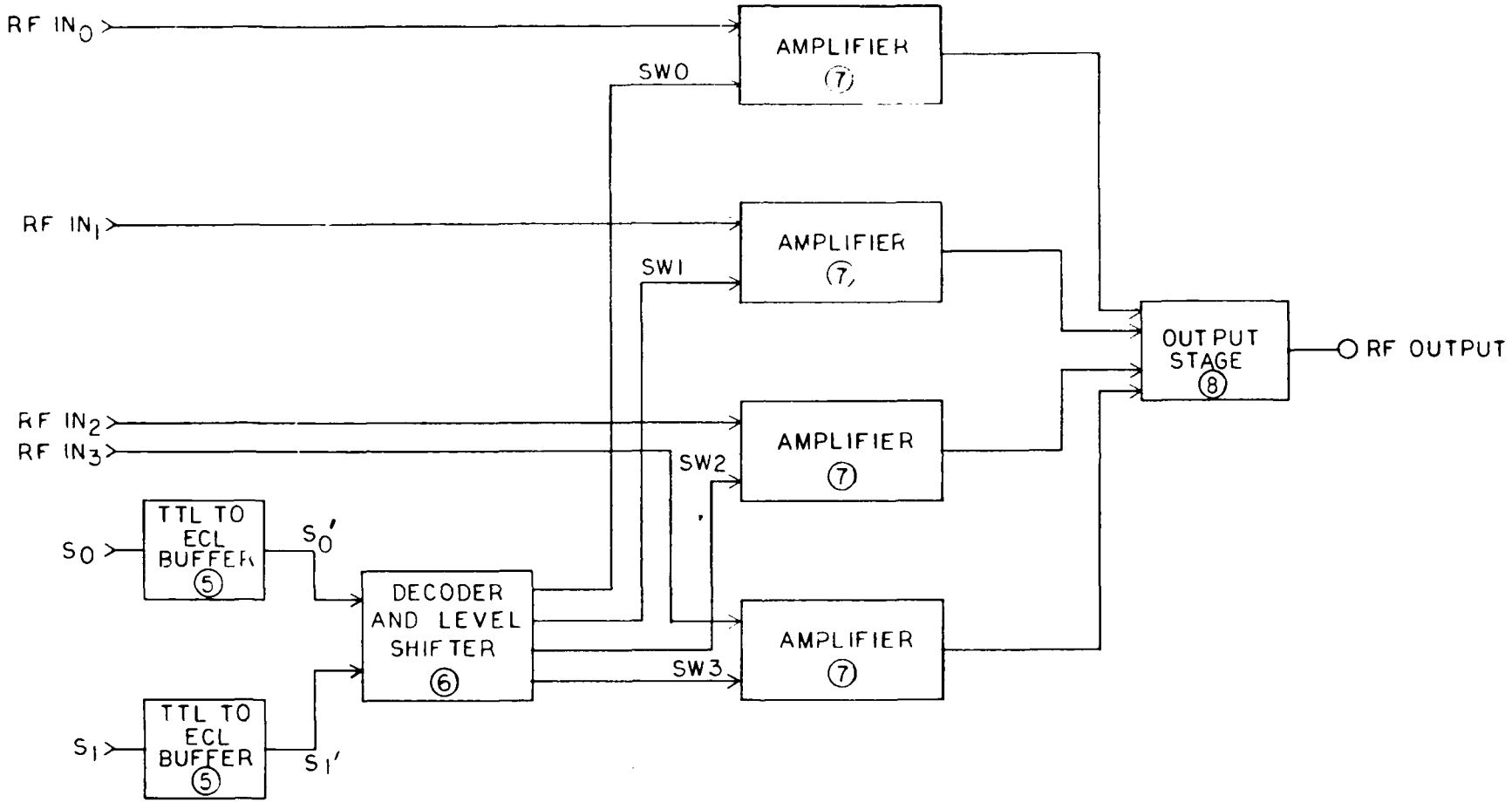
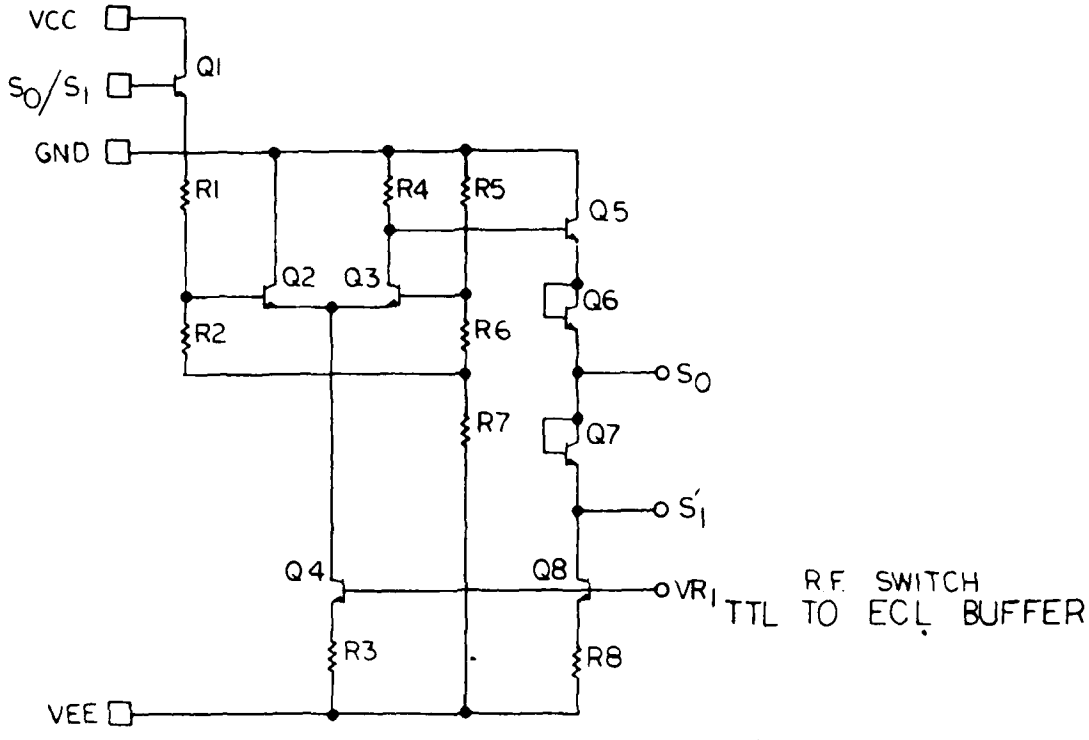


Figure 3-28.

RF SWITCH BLOCK DIAGRAM



RESISTOR VALUES ARE IN OHMS AT 200 OPS

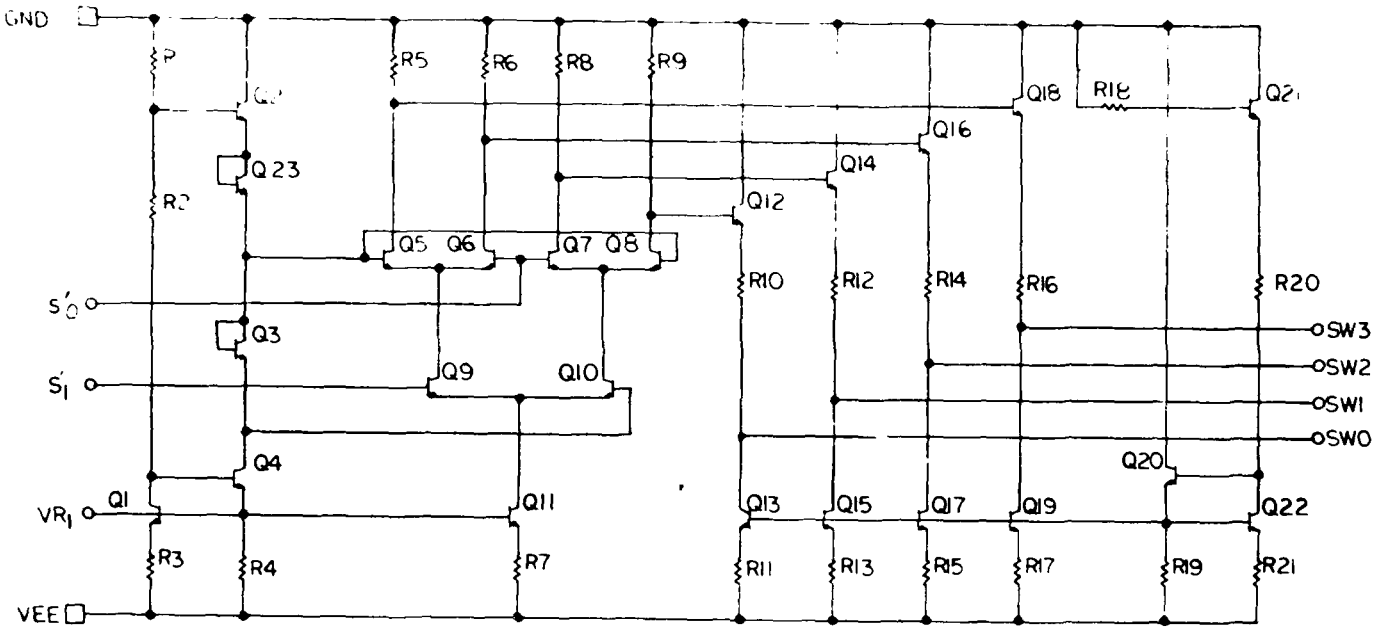
1. R1=2.4K
2. R2,R6=1.2K
3. R3,R7 R8=1K
4. R4=2K
5. R5=1.8K

NOTES:

1. VEE=-5.0VDC
2. ALL TRANSISTORS ARE 2TIL12W4
3. VCC=+5.0 VDC
4. P_D = 20mw

Figure 3-29.

RF SWITCH TTL TO ECL BUFFER



RESISTOR VALUES ARE IN OHMS AT 200 OPS.

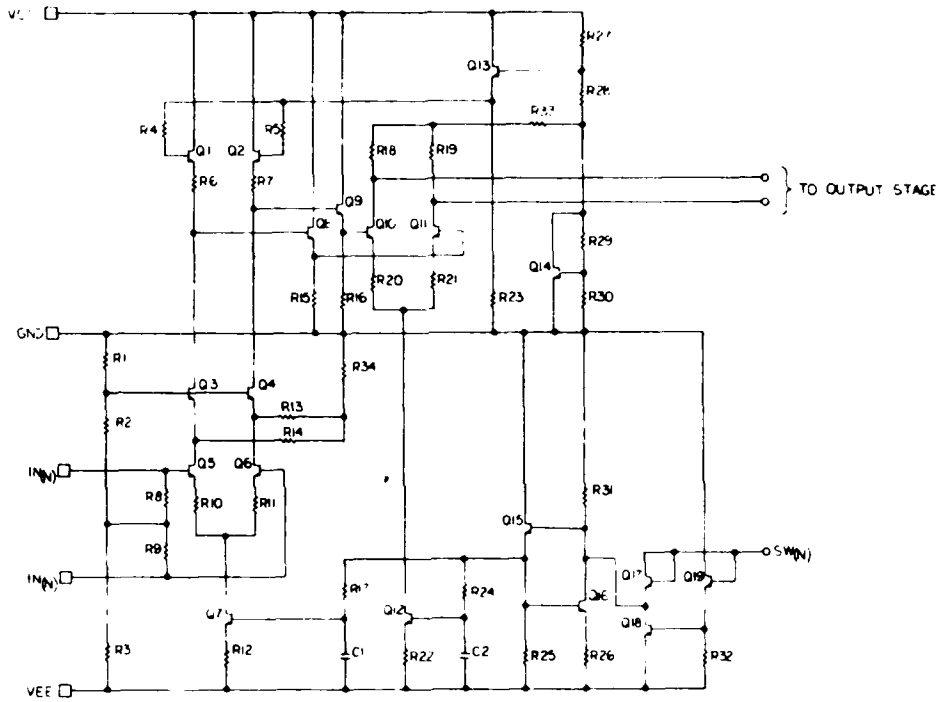
1. R1,R3=800
2. R2=5.28K
3. R4,R19 = 24K
4. R5,R6,R8,R9,R18=1200
5. R7=600
6. R10,R12,R14,R16 = 4.66K
7. R11,R13,R15,R17,R21 = 475
8. R20=5.0K

RF SWITCH
DECODER AND LEVEL SHIFTER

NOTES:
1. VEE=-5.0 VDC
2. ALL TRANSISTORS ARE 2TIL12W4
3. P_D = 23.0 mw
4.

S_0	S_1	SELECT
0	0	SW0
0	1	SW3
1	0	SW1
1	1	SW2

Figure 3-30. RF SWITCH DECODER AND LEVEL SHIFTER



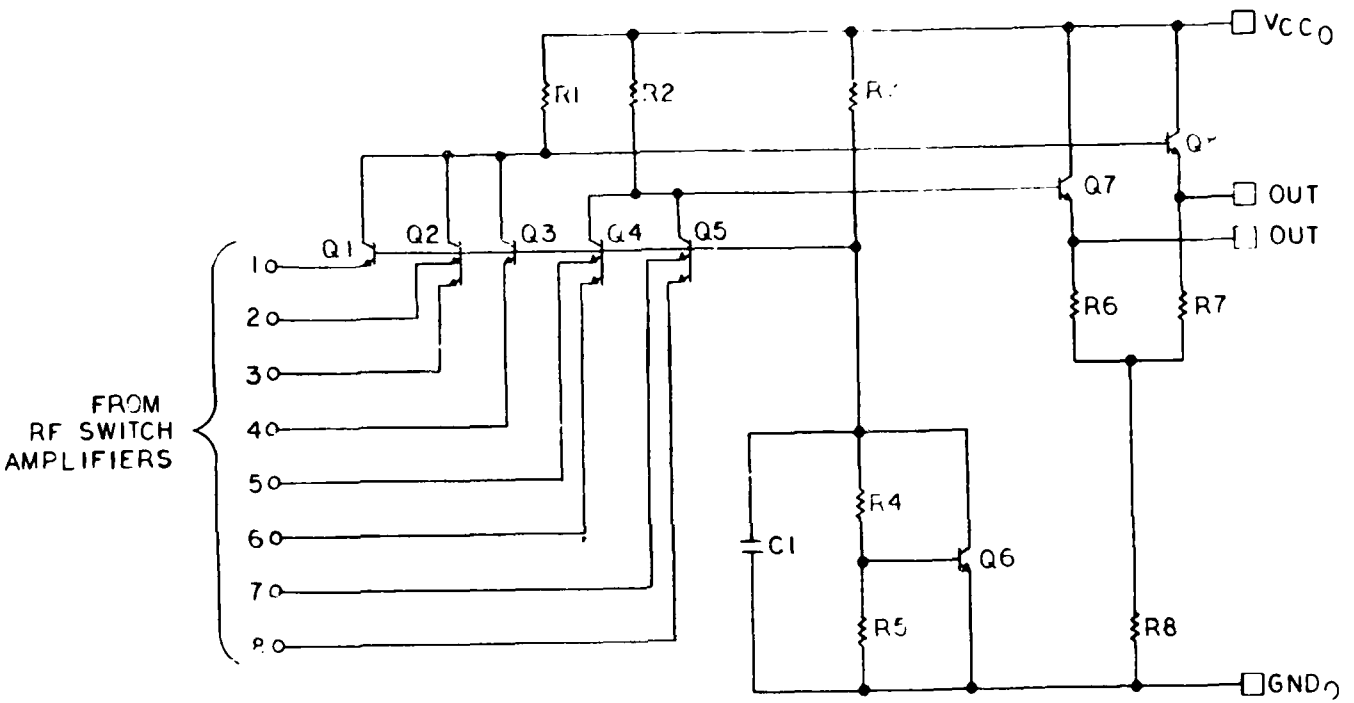
RESISTOR VALUES IN OHMS AT 25° OPS

1 R1 R17, R24 = 400
2 R2 = 3.6K
3 R3 = 3.5K
4 R4 R5 = 1200
5 R6 R7 = 250
6 R8, R9 R 5 R16 R13 R14 = 1K
7 R10, R11, R20, R21 = 30
8 R12 R22 = 200
9 R18 R19 R30 = 5K
10 R23 = 4K
11 R25 = 500
12 R26 = 900
13 R27 = 13K
14 R28 = 350
15 R29 = 4.2K
16 R31 = 5.6K
17 R32 = 16K
18 R33, R34 = 50K
19 C1, C2 = 24 pf

RF SWITCH AMPLIFIER

NOTES
1 VEE = -5.0 VDC
2 ALL TRANSISTORS ARE 2N1132 OR 4
3 CAPACITORS ARE BURIED LAYER TO ISOLATION DIODES
4 VCC = 5.0 VDC
5 INPUT PADS ARE 4 MILS IN DIAMETER
6 PD = 57.6 mW

Figure 3-31. RF SWITCH AMPLIFIER



RESISTOR VALUES ARE IN OHMS AT 200 OPS

R1,2=200
R3=1.65K
R4=4.2K
R5,8=1.5K
R6,7=1K
C1=2.0 PF

RF SWITCH
OUTPUT STAGE

NOTES:

1. ALL TRANSISTORS ARE 2TIL12W4
2. VCC_O=5.0+VDC
3. CAPACITOR IS BURIED LAYER TO ISOLATION DIODE.
4. OUTPUT PADS ARE 4 MILS IN DIAMETER.
5. P_D=19.6 mw

Figure 3-32. RF SWITCH OUTPUT STAGE

Figure 3-33 below shows the ADM-1 block diagram.

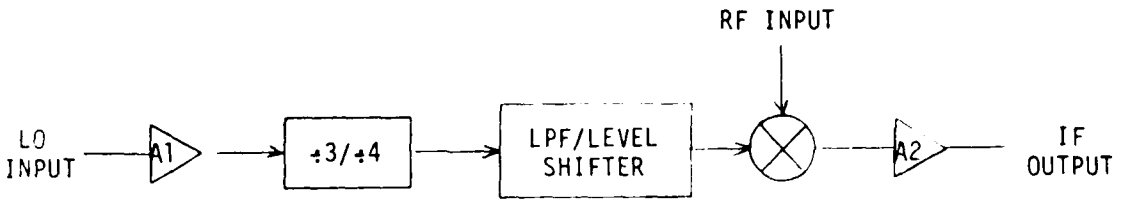


Figure 3-33. ADM-1 BLOCK DIAGRAM

Figure 3-34 shows a photograph of the originally proposed ADM-1 chip. All functional modules shown in the block diagram of Figure 3-33 were fabricated and interconnected on this single 100 x 75 mil silicon chip.

Table 3-5 gives detailed preliminary electrical specifications of the individual ADM-1 functional circuits. Because a differential circuit design philosophy was implemented for each of the functional units of the ADM-1, a similar interconnection concept between chip modules was matinatined. This concept provided a higher level of flexibility in that it provided for the ability to reduce even-order mixer harmonics; however, it complicated the task of characterizing individual module performance. As a result, the ADM-1 chips, as first fabricated, became characterized in a pass/fail fashion, incapable of being reworked as a serviceable unit.

Technical deficiencies in unit performance encountered during early evaluation testing demonstrated the need to examine each module as a stand-alone unit. This feature would allow the establishment of baseline performance data under synthesizer drive conditions prior to interconnection as a final ADM. During this mode of evaluation, separately packaged versions of each block of the ADM-1 module were tested. It was determined that two units were defective from either an electrical design standpoint or from errors encountered in the photolithographic-mask fabrication processes.

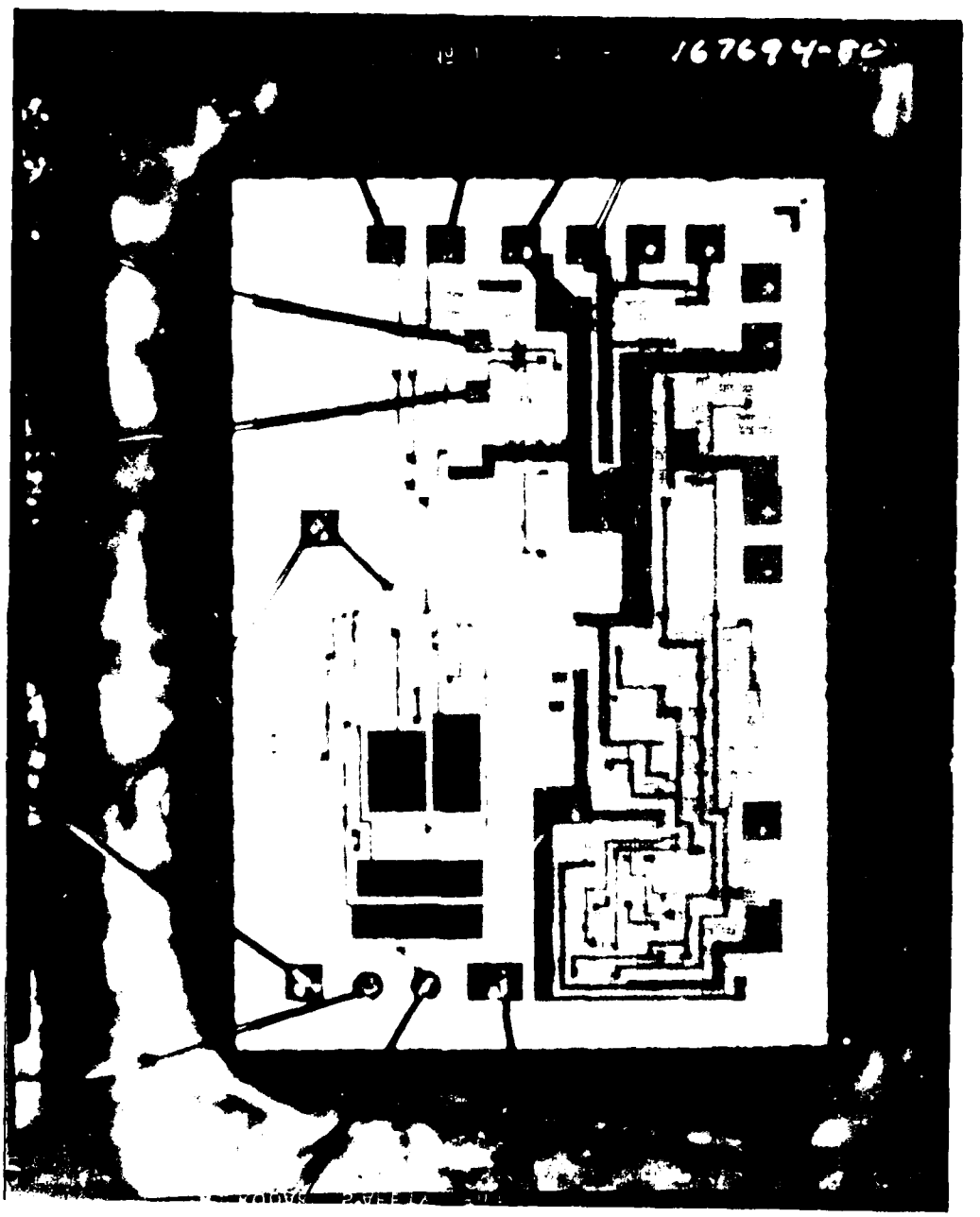


Figure 3-34. ADM-1 CHIP PACKAGE

Table 3-5. ADM CIRCUIT SPECIFICATIONS

Circuit	Parameter	Specification
AMP - A_1	Frequency	480-766 MHz
	Output Voltage	400 mV peak
	Input Power	$\geq$ -22 dBm
	Input VSWR	$\leq$ 2:1
	Load Capacitance	$\leq$1.2 pf
	Output Quiescent Level	2V
Divider	Frequency	640-766 MHz (÷4) 480 MHz (÷3)
	Output Swing	200 mV
	Output Quiescent Level	4.8V
LPF/Level Shifter	Frequency	160-192 MHz
	Fundamental Atten.	6 dB
	7th Harmonic Atten.	42 dB
	Output Quiescent Level	-2V
Analog Multiplier	Input Frequencies	160-192 MHz & 480-576 MHz
	Output Frequency	640-768 MHz
	Output Level	10 mV peak
	Output Quiescent Level	2.5V
	Output Impdeance	200 ohms
AMP - A_2	Frequency	640-768 MHz
	Output Power	$\geq$ -15 dBm
	Output VSWR	$\leq$ 2:1
	Output Compression Point	>-8 dBm

The "fix" for the input amplifier problem was to replace the fabricated Al portion of the ADM-1 chip with an external RFCS-1 RF amplifier chip. The existing Al amplifier output metal-II lines would be cut with a low power laser, thereby removing the level-shifting outputs to the divider inputs, and the new RFCS-1 amplifier would be wire-bonded onto the ADM chip at the appropriate pad locations. A new bias network would be added external to the package to supply the required +2.0 VDC bias to the divider input stage.

To accomplish the lowpass filtering, found to be the other ADM-1 design deficiency problem associated with the LPF/level shifter circuitry, off-chip passive LPF networks were designed. These filter networks were re-designed to attenuate all of the divider harmonics present above 162 MHz, by greater than -50 dBc. An additional bias network, similar in design to that mentioned above, was added external to the package to apply -2.0 VDC bias to each of the mixer LO input ports, thereby replacing the level shifting circuitry.

In addition to implementing the hardware modifications to the input amplifier (RFCS-1), external LPF, and bias networks at the divider and mixer inputs, a separate programmable divider chip was provided. The revised ADM-1 configuration, consisting of three RF-LSI chips as shown in Figure 3-35, provided for individual chip characterization; in the event that piece-part replacement within the single packaged module be required to provide a complete working unit.

Figures 3-36 and 3-37 show the revised ADM-1 packaging scheme. Note the placement of each of the three RF-LSI chips, RFCS-1, ÷3/÷4 divider, and Mixer A2, within the 24-pin flatpack carrier.

3.4.1.2.1 RFCS-1

The input amplifier in the LO chain of the modified ADM-1, as seen in Figure 3-36, is similar to the switch amplifier found in the SP4T switch. Bias voltages for the RFCS-1 of the ADM-1 were extended to cover a 15 volt dynamic range, thereby providing higher saturated output power. An increased in-band gain as well as flat passband response is obtained by grounding the current adjust input of the device. Typical performance data for the RFCS-1 amplifier, obtained under differential input drive and output conditions, is given in Table 3-6.

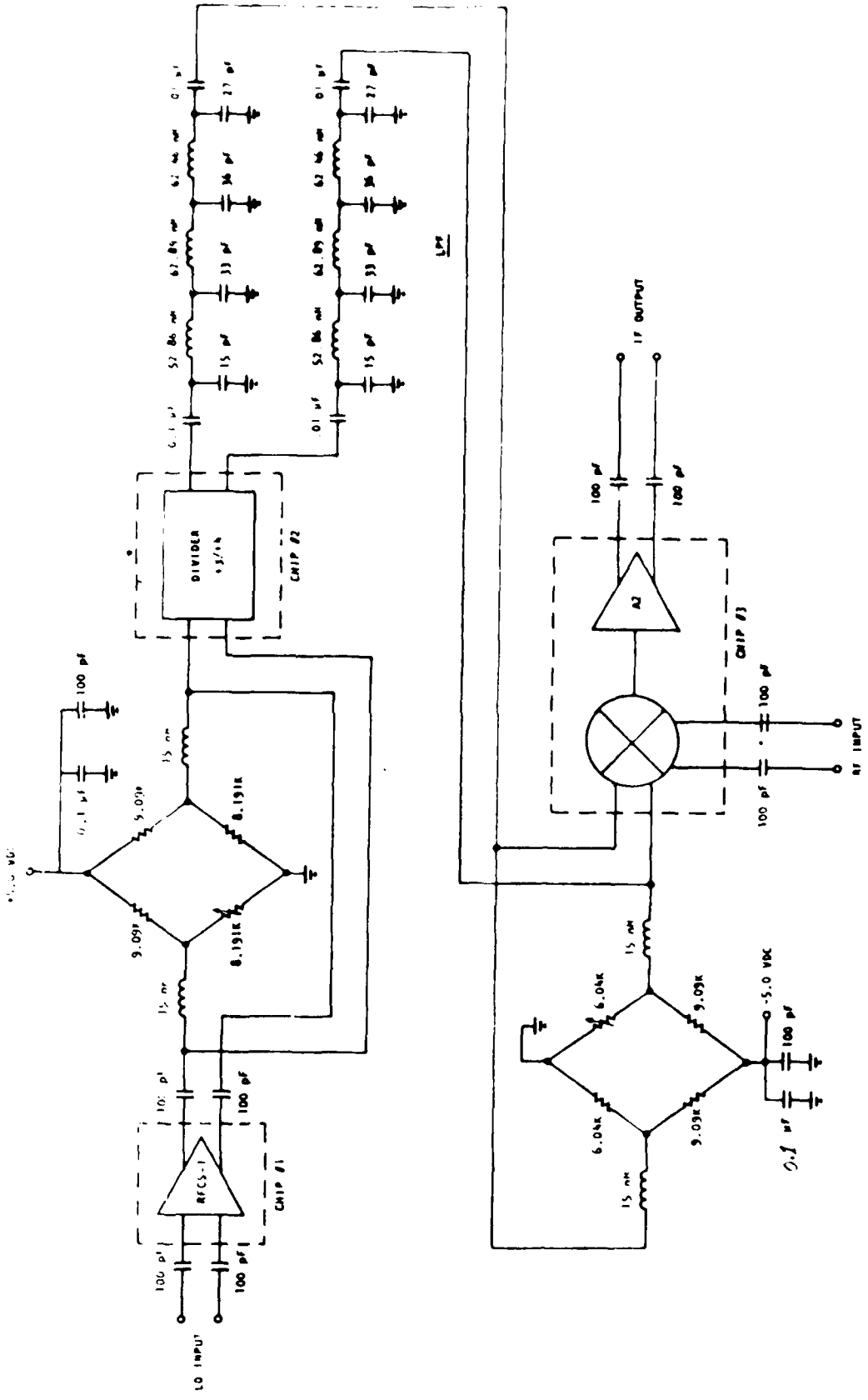


Figure 3-35. REVISED ADM-1 CIRCUIT

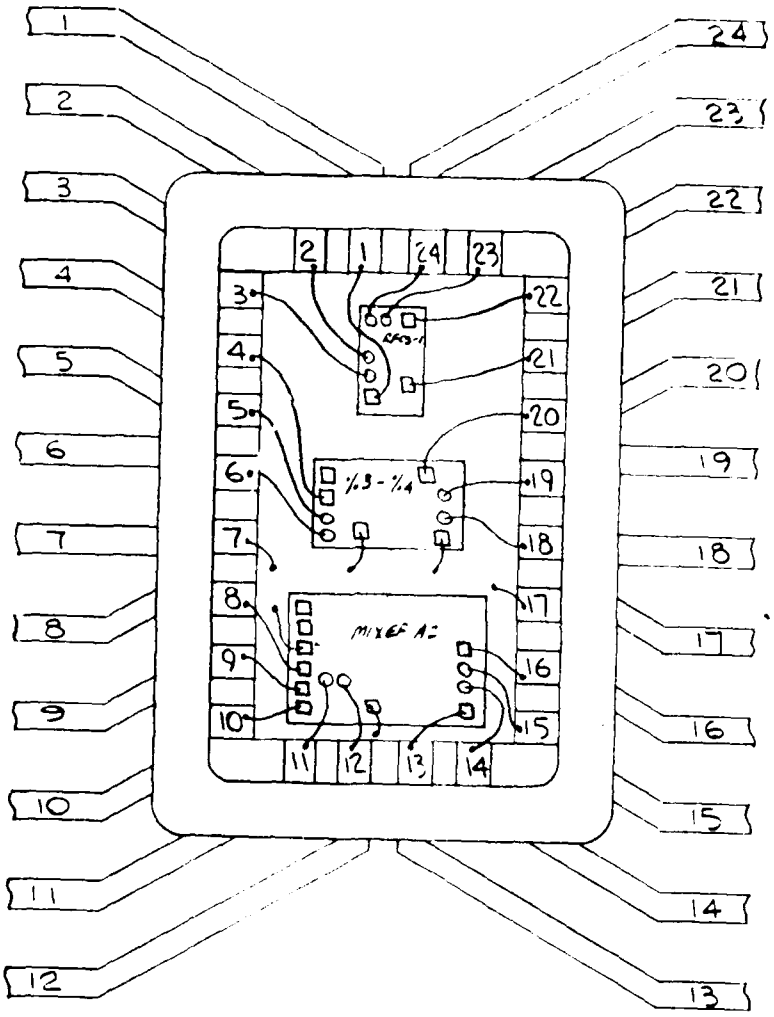


Figure 3-36. ADM-1 PACKAGE

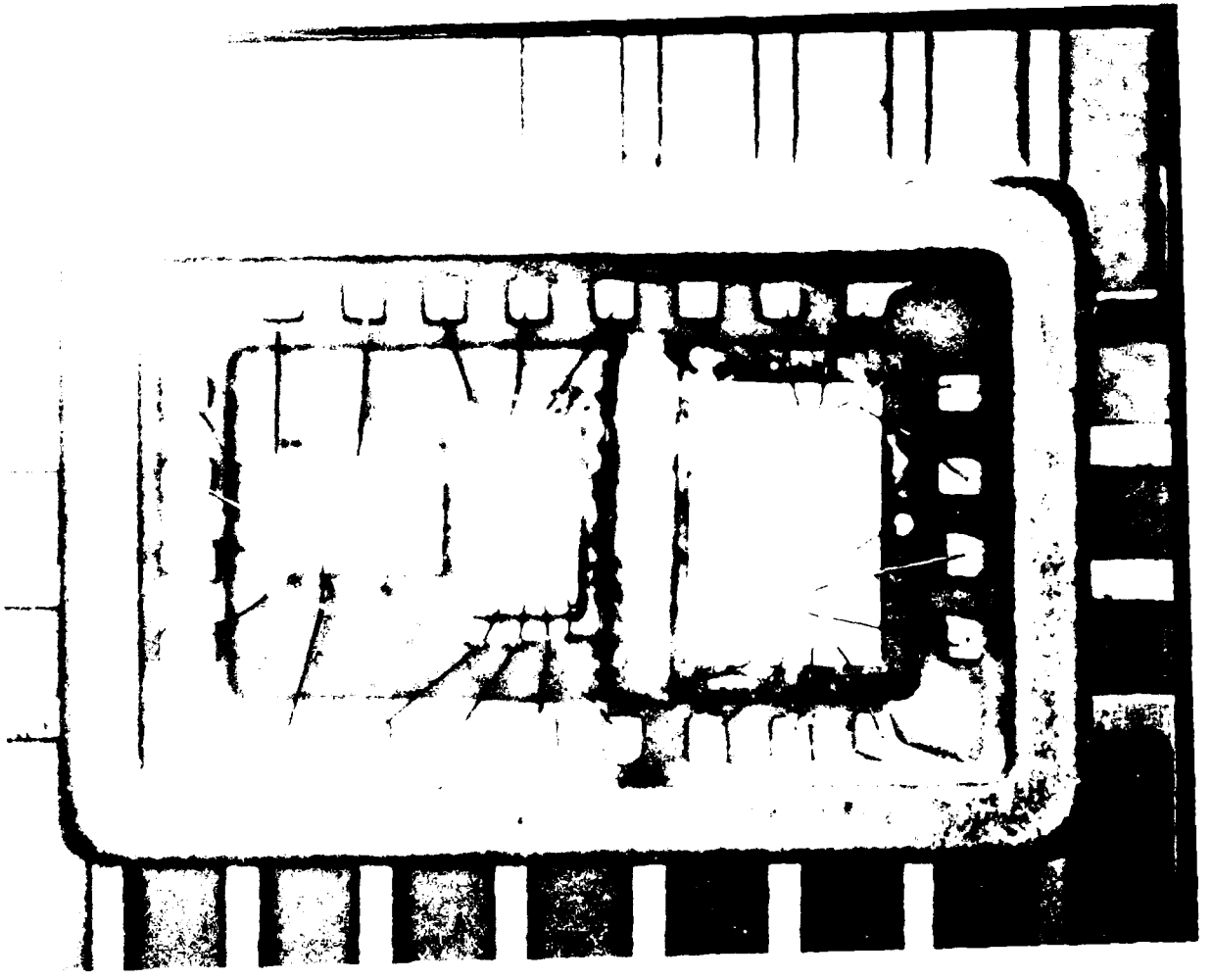


Figure 3-37. REVISED ADM-1 PACKAGING SCHEME

Table 3-6. TYPICAL RFCS-1 PERFORMANCE

P_{SAT}	-3.0 dBm
Gain at f_o	15.5 dB @ 700 MHz
3 dB Gain Bandwidth	300 MHz
DC Power Consumption	750 mW

A schematic of the RFCS-1 circuitry is seen in Figure 3-38.

3.4.1.2.2 Programmable Divider (÷3/÷4)

Before the electrical specifications and design considerations are detailed for the programmable divider circuitry, some clarification should be given regarding the data presented in subsequent test. The data sheets which outline divider performance and figures given showing divider output spectral content were taken from circuitry developed utilizing divider operation in a ÷4 mode, except where ÷3 operation is specified. The performance of the divider circuitry, in terms of harmonic level generation, is similar in both the ÷3 and ÷4 modes, in that subsequent circuitry developed to remove undesirable divider output harmonics for the ÷3 mode of operation has been scaled in frequency to achieve similar stopband performance to data presented for the ÷4 mode. Similarly, passband frequency translation has been incorporated to achieve the required ÷3 operation, thereby providing a mixer LO port drive spectrum consistent with the ÷4 spectrum achieved after proper off-chip filtering. The required off-chip filter design for attainment of ADM-1 performance which minimizes spurious product generation is, however, described in the LPF section of the text, and the distinction between ÷4 spectral performance and ÷3 performance is therefore highlighted.

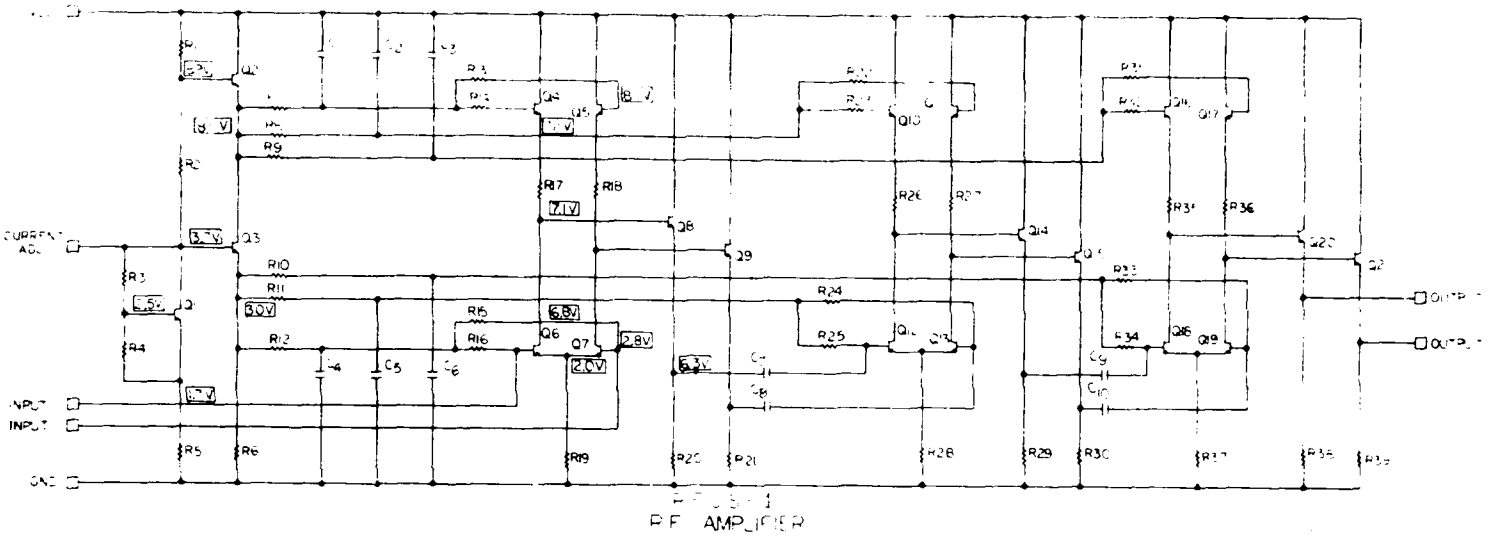


Figure 3-38. RF AMPLIFIER

The programmable ÷3/÷4 uses low level differential logic, which interfaces well with the rest of the circuitry. A block diagram of the divider is shown in Figure 3-39. The logic is somewhat unconventional, but allows the counter to be implemented with gates with only two inputs, which permits the full speed capability of the differential logic to be realized. This insures that 800 MHz divider operation can be routinely achieved without the need to select chips and possibly suffer a yield loss. The additional AND gate shown on the output is optional; in the ÷3 mode, it provides a 50% duty cycle output rather than the 1/3 or 2/3 duty cycle normally obtained from a ÷3, and thus suppresses the DC and even harmonic components fed to the mixer.

Typical performance data for the divider circuitry, obtained while being driven differentially from the RFCS-1 amplifier (at -30 dBm input), is given in Table 3-7. It should be noted that due to the differential divider output arrangement, Table 3-7 data was measured with the lowpass filters in place at the divider outputs.

Table 3-7. TYPICAL DIVIDER PERFORMANCE DATA

DC Power Consumption	$\leq$250 mW
Input Trigger Threshold	$\geq$-18 dBm
F_{IN} (÷4)	600-800 MHz
F_{IN} (÷3)	450-550 MHz
P_{OUT}	$\geq$-17.0 $\pm$1.5 dBm
F_{OUT}	120.0 - 191.5 MHz
Input Bias (V_{Bias})	+2.0 VDC

Figure 3-40 shows typical divider output spectral data (÷4 mode). Test conditions for this case are as before, RFCS-1 driving divider with -30 dBm at LO input, except a 180° hybrid coupler is used to convert the differential output configuration to a single-ended mode, presenting a 50 ohm output for measurement. Bias "tee" networks between the divider outputs and the coupler input ports restrict divider output stage bias voltages to the test fixture circuitry, and allow the $F_{LO}/4$ spectrum to pass through to the spectrum analyzer for measurement. No lowpass filters are present, so as to allow measurement of the divider harmonics present in the LO passband from 640-766 MHz. From Figure 3-56, for an LO input signal at 640 MHz, $F_{LO}/4$ is seen as a signal at 160 MHz and -18.1 dBm in level at the divider output. The principle harmonic of the 160 MHz baseband signal seen at 480 MHz is only -26 dBc, and the LO signal seen at 640 MHz is -31.3 dBc. Again, similar harmonic levels are present for ÷3 operation.

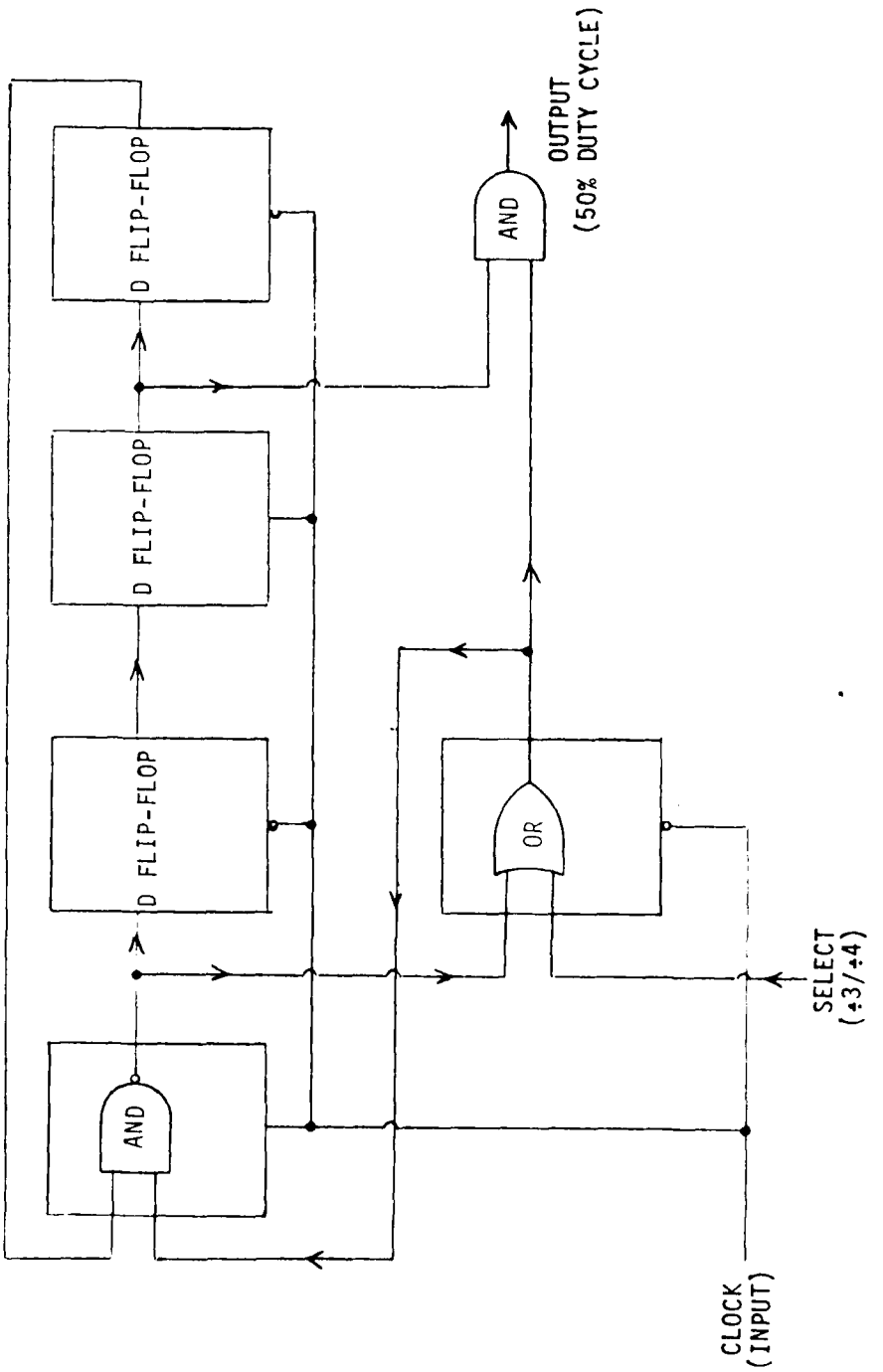


Figure 3-39. ÷3/÷4 WITH 50% DUTY CYCLE OUTPUT

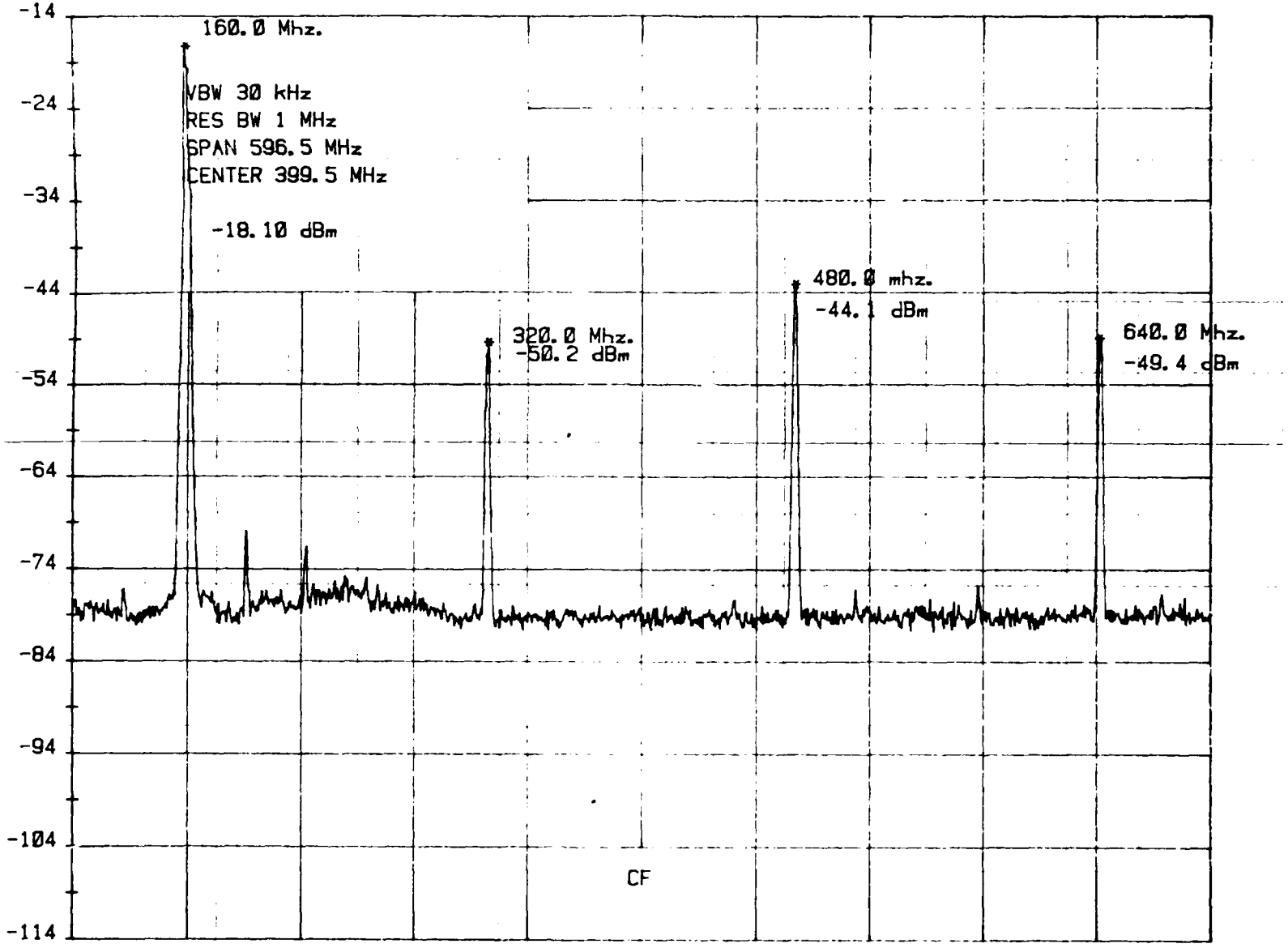


Figure 3-40. FREQUENCY SYNTHESIZER S/N 01 ADM-1 #3 DIVIDER OUTPUT
(1280 MHz SELECTED OUTPUT WORD)

From the data given by Figure 3-40, it is apparent that an additional lowpass filter stopband attenuation of $\geq$35 dB be imparted at the second-order and higher harmonics of the baseband divider output frequencies if a minimum -60 dBc spurious requirement is to be met. This, of course, assumes that the ADM-1 mixer conversion gain will not appreciably raise any harmonic-in-origin spurious signals generated when the divider output spectrum is mixed with the selected SP3T signals.

Figure 3-41 shows the programmable divider schematic.

3.4.1.2.3 Off-Chip LPF

The original implementation of the ADM hardware included a lowpass filter/level shifter network to follow the divider output stage. The proposed design consisted of a series emitter-follower/diode level shifter and differential stages with diode peaking. The design provided for a 7-stage cascaded design of single-pole networks with a 600 MHz corner frequency, rolling off to give greater than 40 dB of attenuation at the 7th harmonic at 1120 MHz. However, as early speculation had pointed out, realization of such a design would be difficult to produce reliably in monolithic form due to component tolerances.

Initial studies conducted to examine spurious requirements impacted by the proposed RF-LSI design philosophy indicated that in-band spurs, present at a level as high as -17 dBc, might be generated at the mixer output. The impact of these in-band tones was determined to be the worst case when evaluating the 7th harmonic of the divider output. However, as Figure 3-40 has shown, baseband harmonics as high as -26 dBc are present at the divider output, due in fact to the nature of the squarewave output of the digital divider.

In an attempt to remove all even and odd ordered harmonics present at the divider output, and pass the LO/3 baseband signals, an off-chip lowpass filter design was implemented. The circuitry fabricated on the ADM-1 substrate to provide the LPF/level shifting function was therefore cut away from the remaining mixer/A2 portion of the chip, leaving only those two remaining functional sections on to be used in the modified ADM configuration.

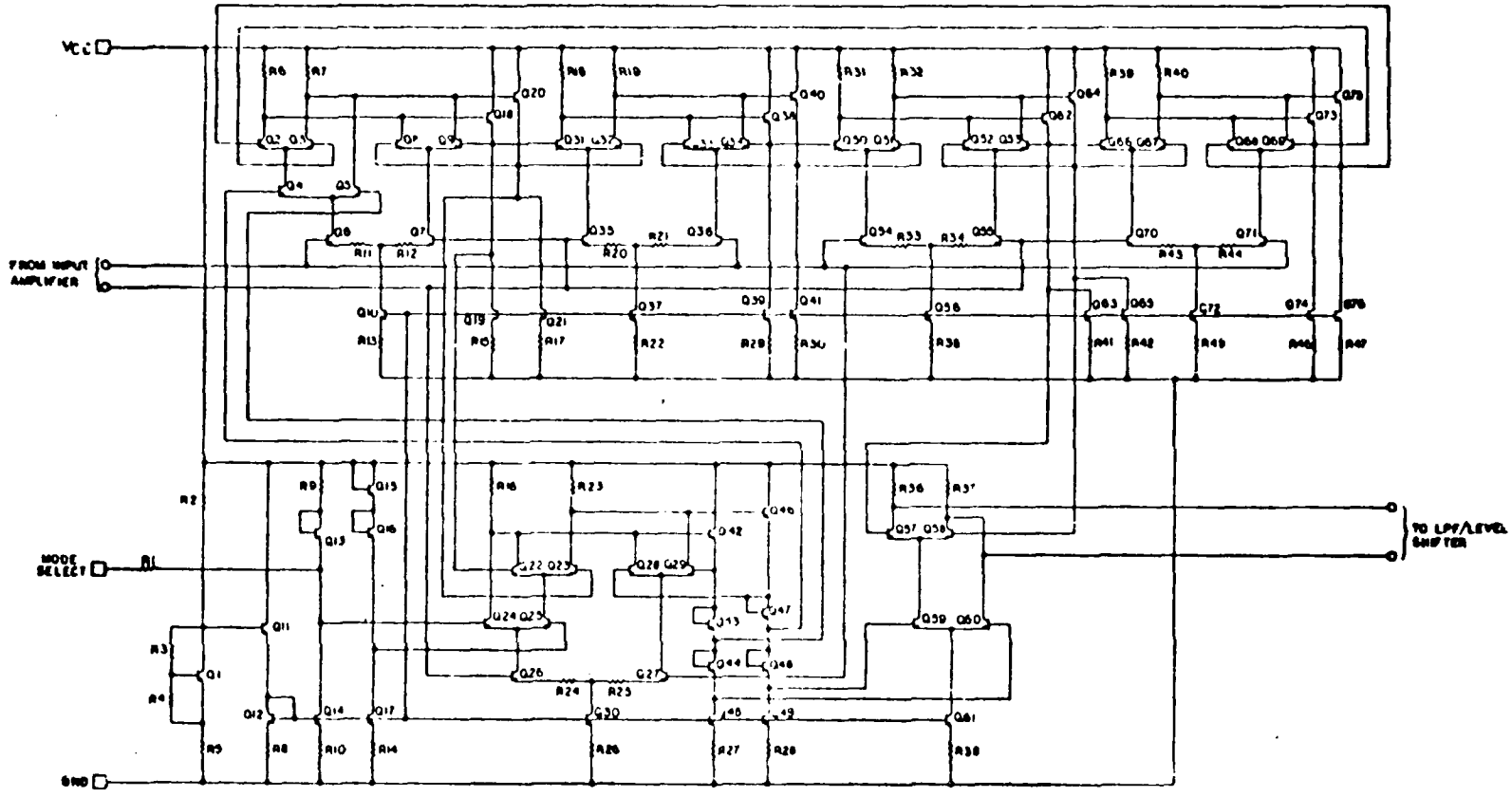


Figure 3-41. ADM-1 DIVIDE BY 3 & 4

The off-chip design consists of a 7th order, Chebychev, 0.1% ripple lowpass design with 0.01 μF coupling capacitors at both input and output. The filter is designed to translate a 50 ohm source impedance, seen looking into the divider output stage, to a 1.28K ohm load presented by the mixer input circuitry. The 3 dB bandwidth was chosen to be 162 MHz, to allow passage of a maximum baseband frequency of 486/3 MHz and allow for fabrication-tuning error. It was desired to provide a minimum of 30 dB of stopband attenuation at the $2F_{LO_{min}}/3$ frequency at 245 MHz, therefore a 7th order Chebychev design was synthesized. Figure 3-42 gives the schematic diagram of the filter, while Figures 3-43 and 3-44 are plots of measured breadboard filter passband and stopband data.

Figure 3-45 is a plot of the filter response characterized from 50 to 950 MHz, with a deliverable-hardware filter mounted in a test fixture built specifically for simulating the mechanical mounting processes in the final synthesizer configuration. Note that approximately 52 dB of attenuation was achieved at 324 MHz, 162 MHz from the passband marker. This net 6.5 dB variation in attenuation closest to the divider baseband becomes worst at 450 MHz, where an absolute level of -56 dBc attenuation is achieved. This is compared to the -70 dBc attenuation offered by the breadboard filter at 450 MHz in Figure 3-44.

Due to the edgewise mounting technique employed for mounting of the LPF circuit boards, a less efficient RF ground is provided, the effect of which causes a decrease in attenuation with increasing frequency. However the major task of reducing the divider output harmonics has been satisfied.

3.4.1.2.4 Mixer/A2

In the modified ADM-1 configuration, the functions provided by the mixer and output amplifier (A2) are obtained from the original ADM chip. The fabricated Mixer/A2 circuitry was the only remaining portion of the device found to be functionally adequate, and capable of providing a minimum 5 dB conversion gain to IF signals in the range of 600 to 780 MHz. This gain bandwidth

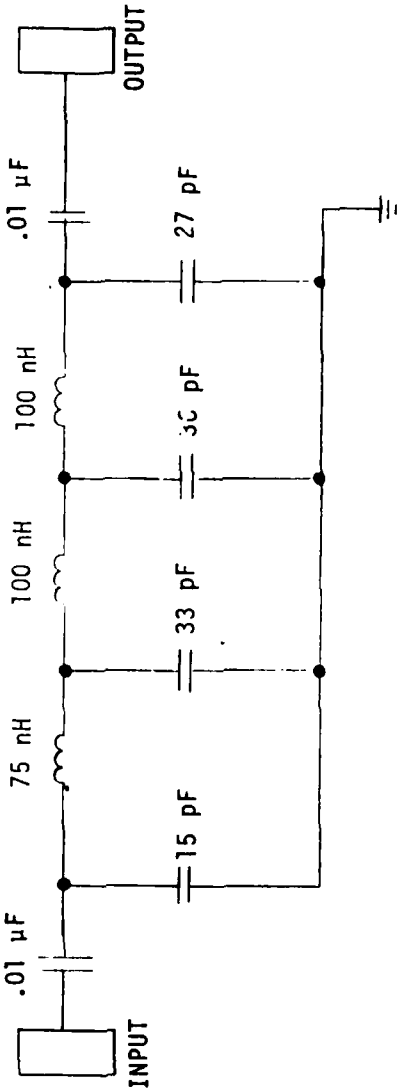


Figure 3-42. FILTER SCHEMATIC

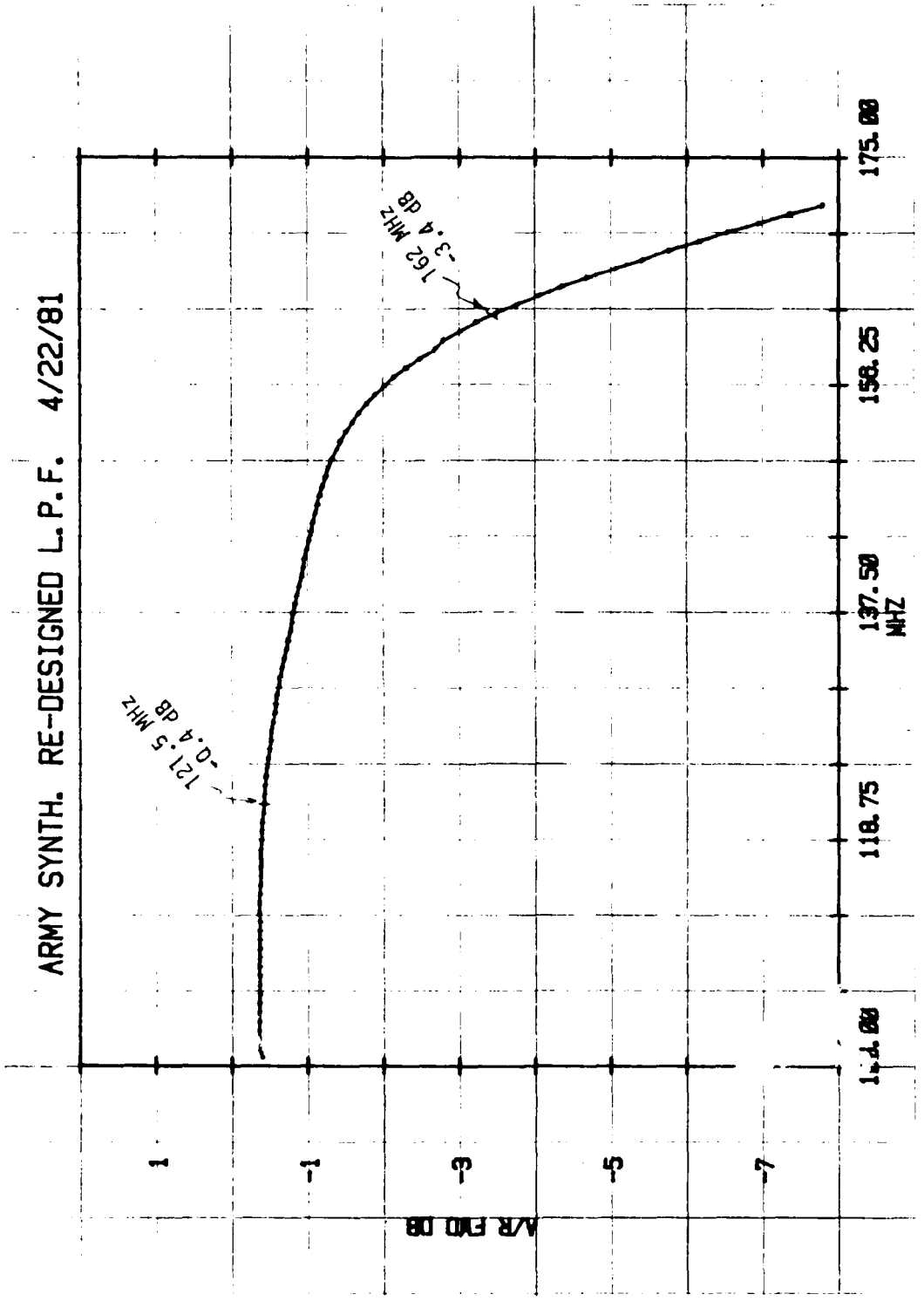


Figure 3-43. MEASURED BREADBOARD FILTER PASSBAND DATA

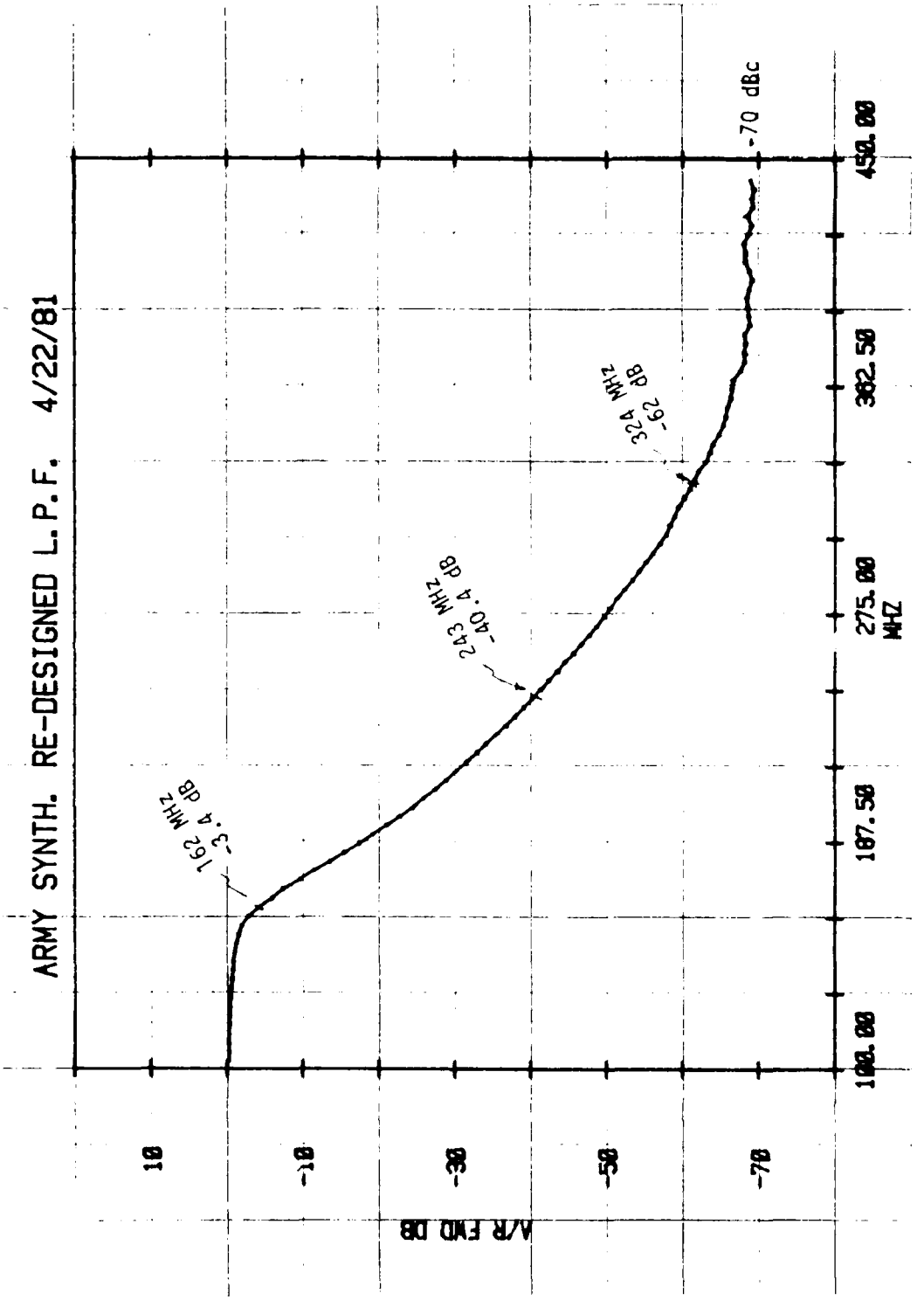


Figure 3-44. MEASURED BREADBOARD FILTER STOPBAND DATA

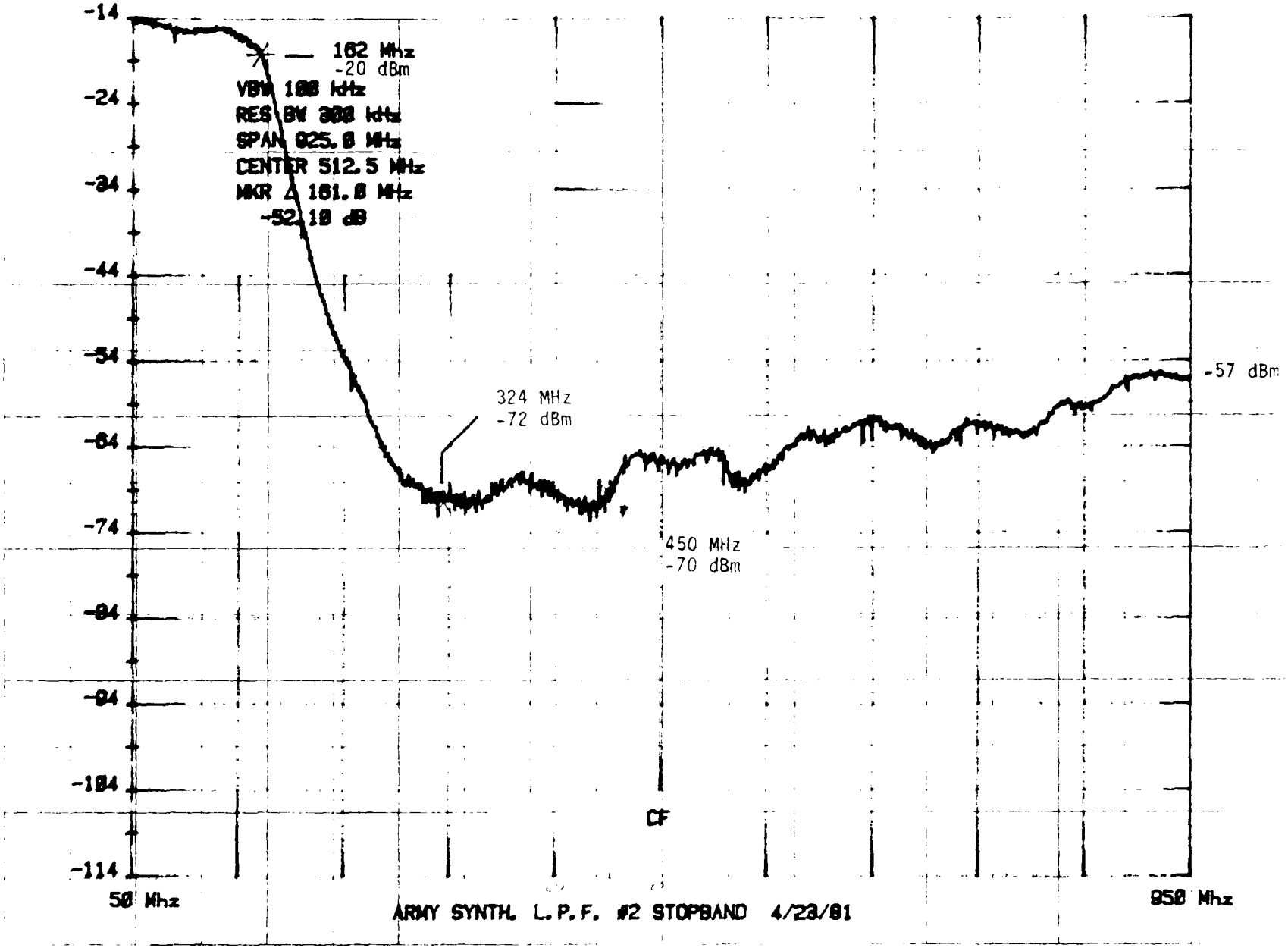


Figure 3-45. FILTER RESPONSE

limitation being applicable to the #4 ADM device of the synthesizer module chain only, due to the difference mode IF produced by the #1-#3 ADM devices. Figures 3-46 and 3-47 show the schematic diagrams of the mixer and output amplifier (A2) of the modified ADM-1 hardware. Table 3-8 below indicates typical measured mixer/A2 conversion gain, as measured under simulated synthesizer drive level conditions at both the LO and RF ports. The LO input ports are driven differentially from the divider, through the lowpass filters, while the RF ports are driven in a single-ended mode, with the undriven input terminated through a coupling capacitor to a 50 ohm load. The IF output port is loaded in a single-ended fashion with the unmeasured output side terminated in 50 ohms also.

From Table 3-8 , the mixer/A2 conversion gain with the divider operating in the ÷4 mode, is shown to vary from 6.25 dB, at an IF frequency of approximately 640 MHz, to a gain of 4.75 dB at an IF frequency of 771 MHz. Maximum conversion gain variation over the IF passband (640-767.5 MHz) is shown to be 1.53 dB. It should be noted, however, that in the divide-by-three mode of operation, an increase in LO drive power of approximately 5.5 dB is required at the divider input to insure generation of the correct IF frequency. This deviation in LO drive requirement is typically accomodated for by raising the minimum LO drive power at the first ADM, and by raising the switch input drive levels so as to produce mixer output IF tone levels high enough to drive successive RFCS-1-Divider stages. In addition, selectively padding the switch output ports to achieve RFCS-1 drive levels on the order of -24 dBm min, will achieve the required divider drive level.

In order to supply proper mixer input bias levels, a bridge-configured network is provided external to the ADM package. This bridge-type of biasing scheme allows for unbalancing the mixer (LO) input port bias voltages to reduce undesirable harmonics produced in the IF passband.

Figures 3-48 and 3-49 show top side and bottom side views of the completed synthesizer module hardware. Figure 3-49 indicates the complexity of the packaging scheme incorporated in mounting both the commercial bandpass filters and off-chip, edgewise mounted, lowpass filters.

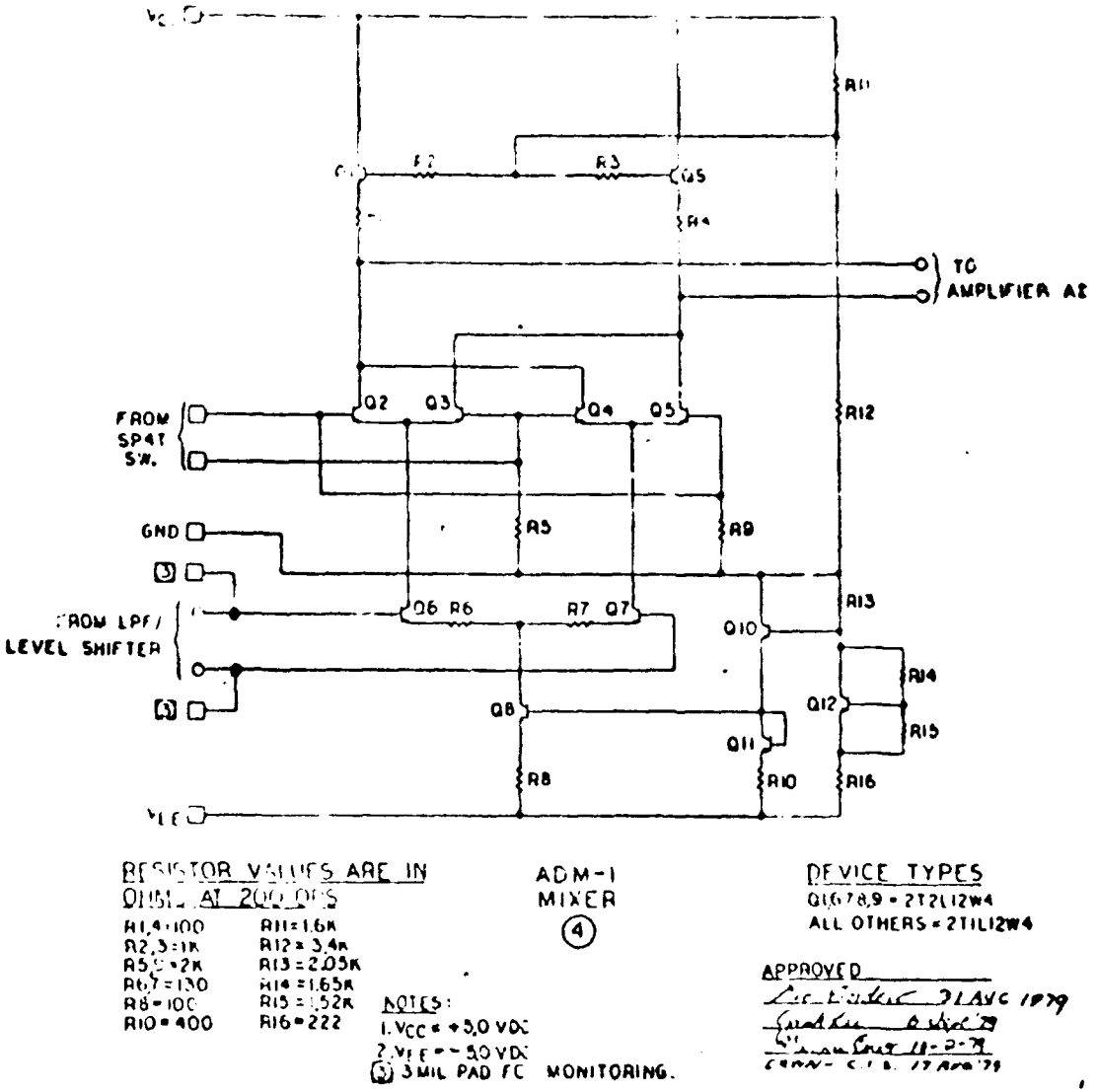


Figure 3-46. ADM-1 MIXER SCHEMATIC

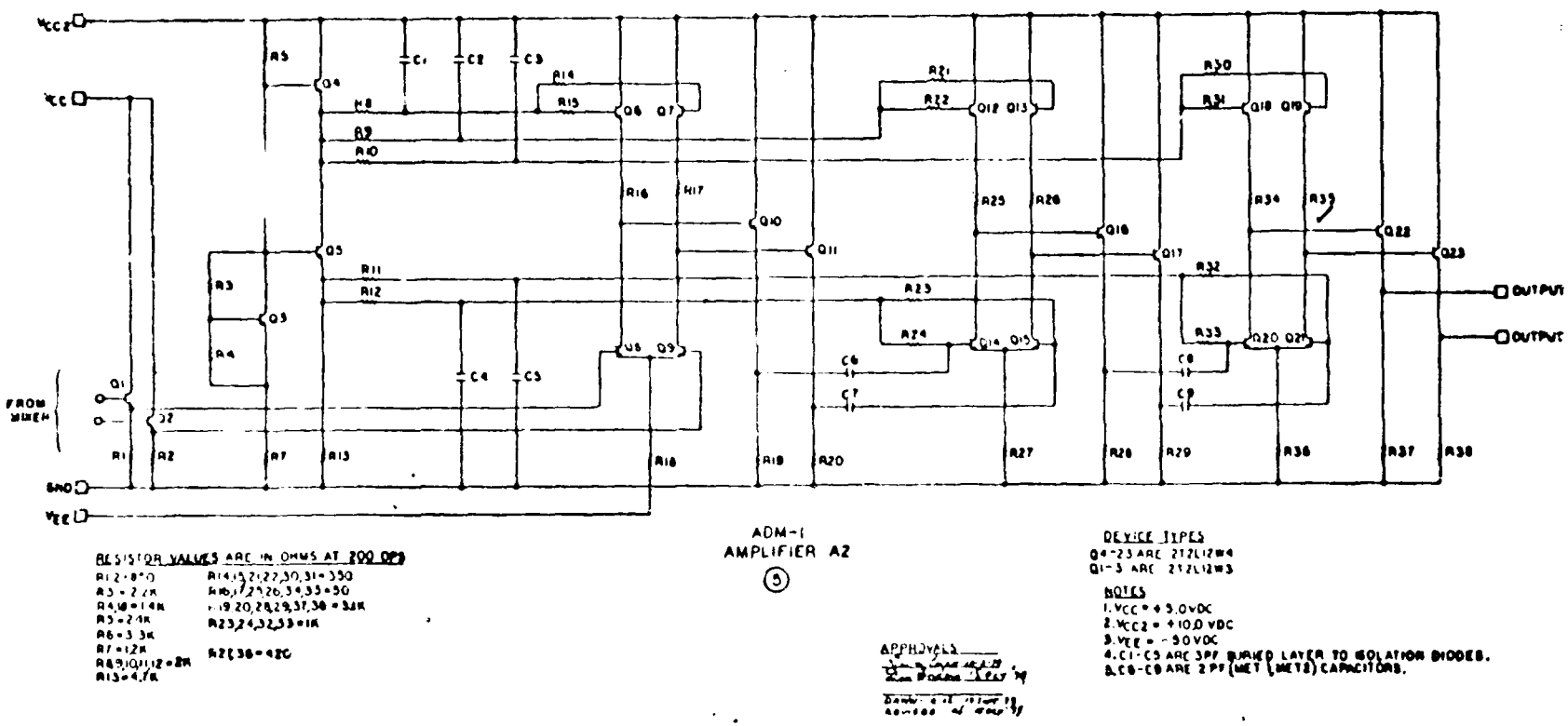


Figure 3-47. ADM-1 AMPLIFIER A2

Table 3-8 TYPICAL MEASURED MIXER/A2 CONVERSION GAIN

Input ±4				Output ±4		
P_{LO} (dBm)	F_{LO} (Mhz)	P_{RF} (dBm)	F_{RF} (MHz)	F_{IF} (MHz)	P_{IF} (dBm)	Conversion Gain (dB)
-17.0	630	-35.0	480	637.50	-28.75	6.25
-17.0	630	-34.70	512	669.5	-29.10	5.60
-17.0	630	-34.73	544	701.5	-28.45	6.28
-17.0	630	-34.85	576	733.50	-30.0	4.85
-17.82	780	-35.0	480	675.0	-28.8	6.20
-17.82	780	-34.70	512	707.0	-28.9	5.80
-17.82	780	-34.73	544	739.0	-29.35	5.38
-17.82	780	-34.85	576	771.0	-30.10	4.75

Input ±3				Output ±3		
P_{LO} (dBm)	F_{LO} (dBm)	P_{RF} (dBm)	F_{RF} (MHz)	F_{IF} (MHz)	P_{IF} (dBm)	Conversion Gain (dB)
-12.12	480	-35.0	480	640.0	-29.55	5.45
-12.12	480	-34.85	576	736.0	-31.00	3.85

$V_{pin\ \#\ 11} = 2.018V$

$V_{pin\ \#\ 12} = -2.014V$

$V_{pin\ \#\ 14} = 4.964V$

$V_{pin\ \#\ 15} = 4.966V$

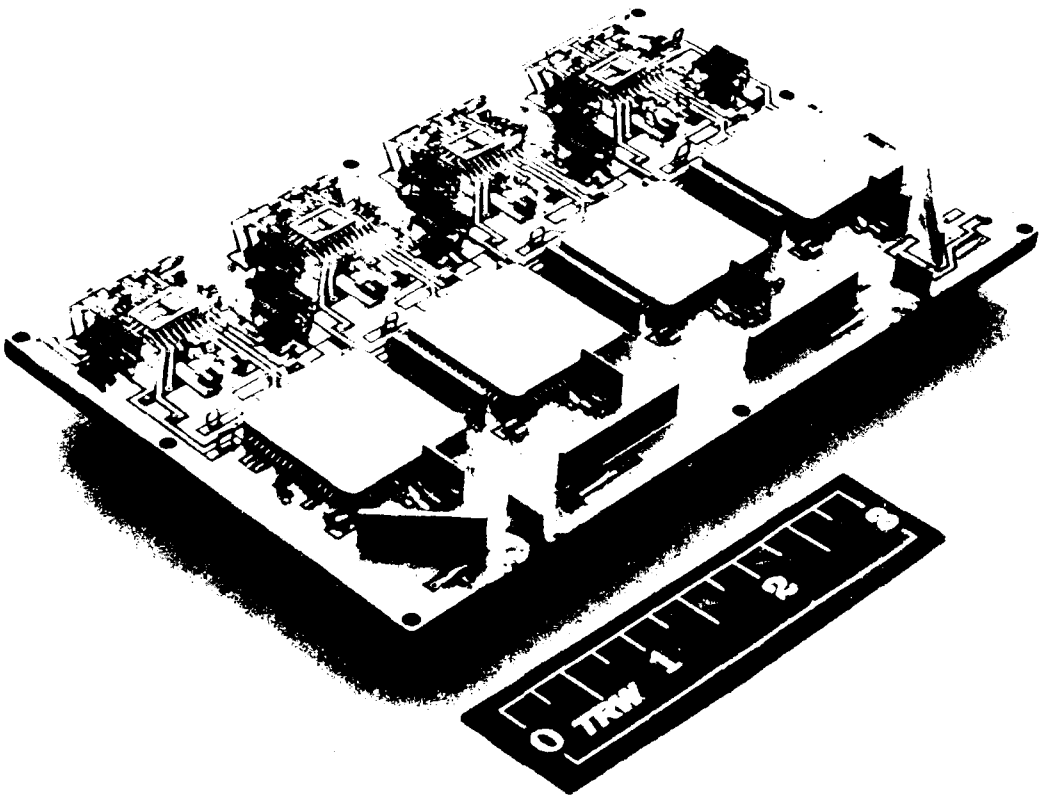


Figure 3-48. SYNTHESIZER MODULE HARDWARE, TOP SIDE VIEW

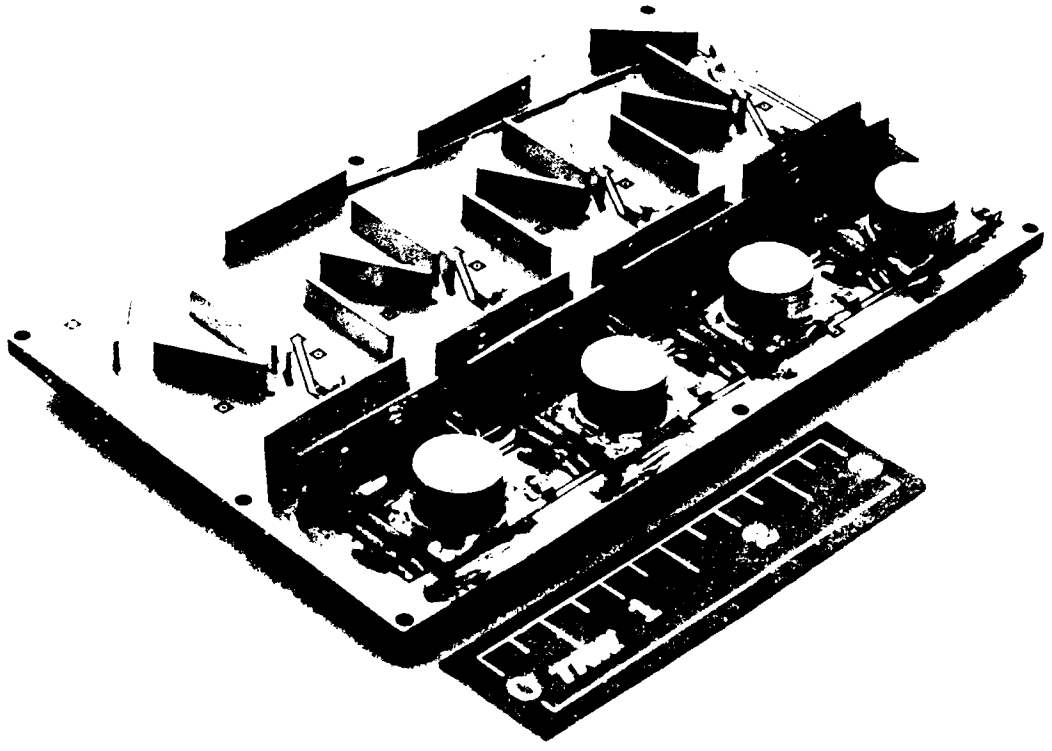


Figure 3-49. SYNTHESIZER MODULE HARDWARE, BOTTOM VIEW

3.5 Output Module

The output module is used to frequency double and amplify the synthesizer board 648-768 MHz, 1.5-MHz step size, output producing an output ranging from 1296 to 1536 MHz, in 3 MHz steps at a saturated power level of +10 dBm. Commercial bandpass filters are incorporated in the design to reduce out-of-band spurs to a level $\leq$ -70 dBc. The bandpass filters are centered at 1416 MHz and have a 330 MHz 3 dB bandwidth, with 1-2 dB of passband insertion loss.

3.5.1 Block Diagram

A block diagram of the output module circuitry is shown in Figure 3-50. The amplifier modules used in the design are commercial wideband RF amplifiers. The X2 circuitry will be described in detail later.

Operation of the circuit can be followed through Figure 3-51, which details gain and power distribution for the module. The input amplifier chain is used to amplify the Synthesizer Module output to approximately +13 dBm at the doubler input. The doubler doubles the input frequency with a conversion loss of approximately 12 dB. The amplifier/filter chain following the doubler amplifies the doubler output to a saturated level of approximately +10 dBm and filters out-of-band spurs. Pads shown throughout the module are used to eliminate mismatches between circuits and thereby assures circuit stability. As Figure 3-51 indicates, an input drive level of -22 dBm (minimum Synthesizer Module output power) produces a saturated +10.3 dBm output. Total noise power at the output will be less than -40 dBm. Table 3-9 below lists typical deliverable output module performance.

Table 3-9 . OUTPUT MODULE TYPICAL PERFORMANCE

Parameter	Expected Performance
f_{IN}	600-800 MHz
P_{IN}	$\geq$-24 dBm
f_{OUT}	1200-1600 MHz
P_{OUT}	+10.0 $\pm$1.0 dBm
Out-of-Band Spurs	<-70 dBc
DC Power Consumption	<3.75W

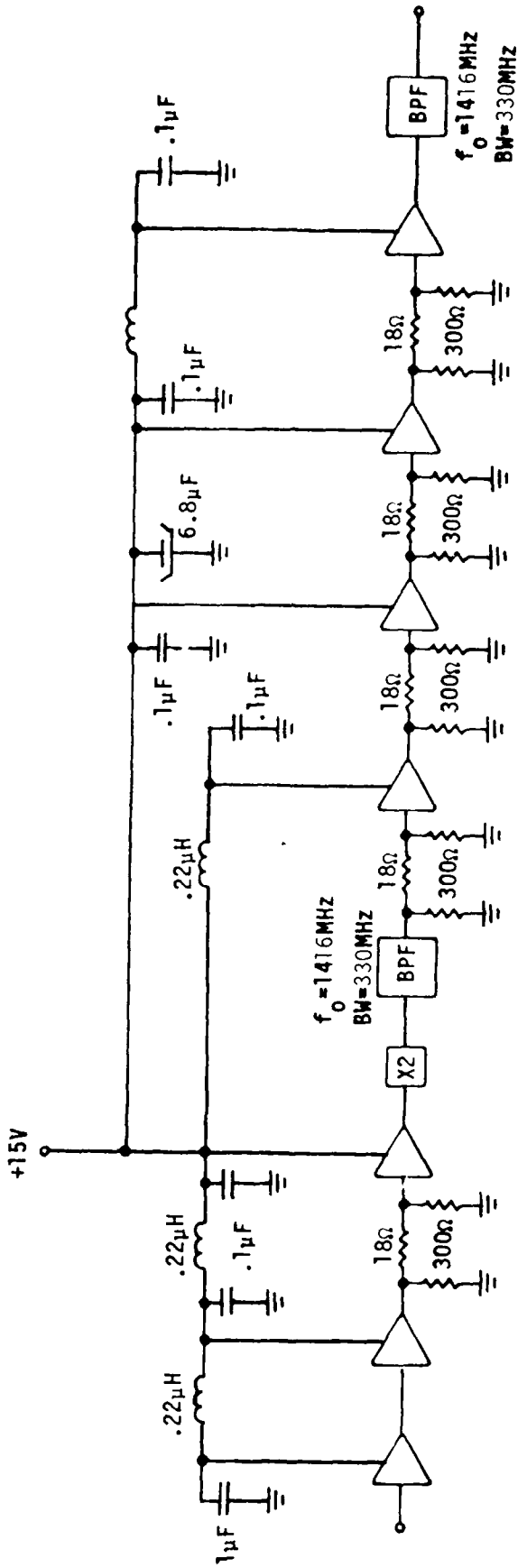
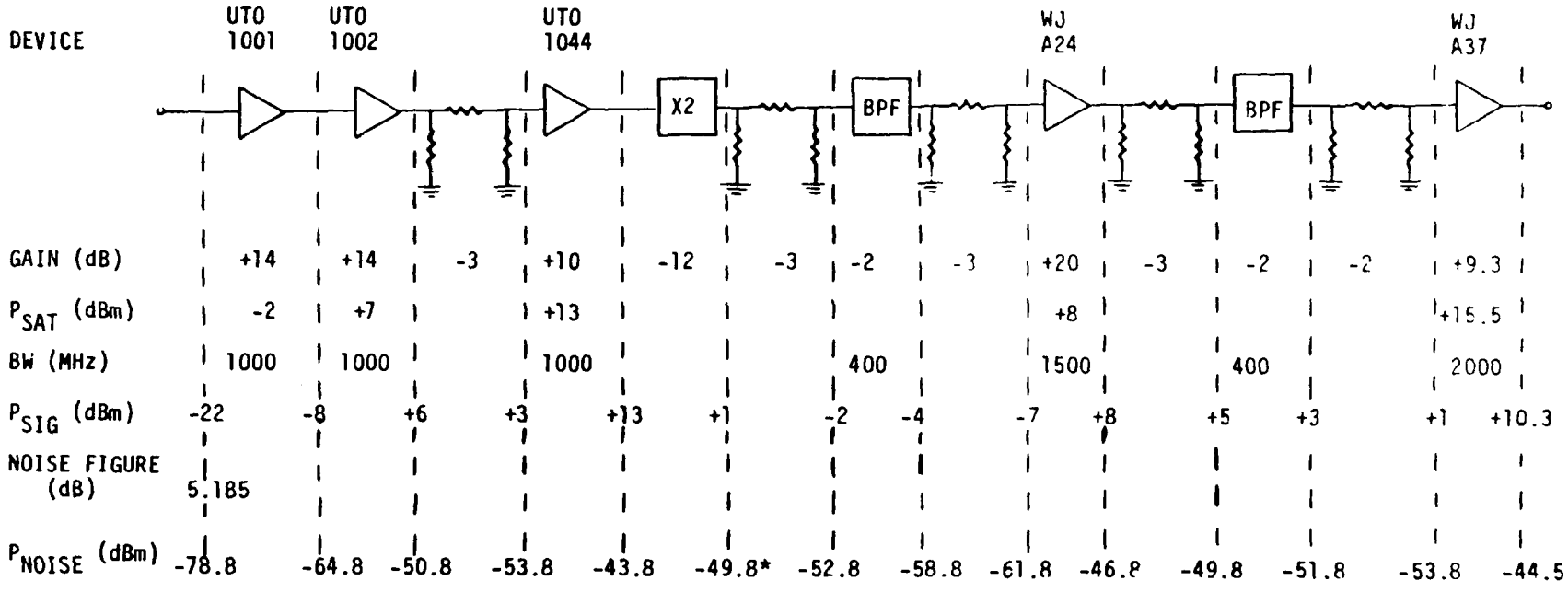


Figure 3-50. OUTPUT MODULE



*Reflects 12 dB conversion loss and 6 dB noise enhancement.

Figure 3-51. OUTPUT MODULE GAIN/POWER DISTRIBUTION

Measured performance of the module is shown in Figures 3-52 and 3-53. Figure 3-52 is a plot of power out (at $2f_o$) vs power in (at f_o). The plot indicates that input power in excess of -28 dBm will produce a saturated output. The data shown was measured at 1416 MHz. Figure 3-53 shows frequency response of the module. Input drive for this data was -25 dBm. The plot indicates that output power is flat to within $\pm$0.5 dB over the 1296 MHz to 1536 MHz frequency range. Figure 3-54 is a plot of the output module wideband frequency response for a single 708 MHz input at -25 dBm. Note that the output module noise floor is measured to be approximately -55 dBc, within the passband of the output filters, and -65 dBc out-of-band.

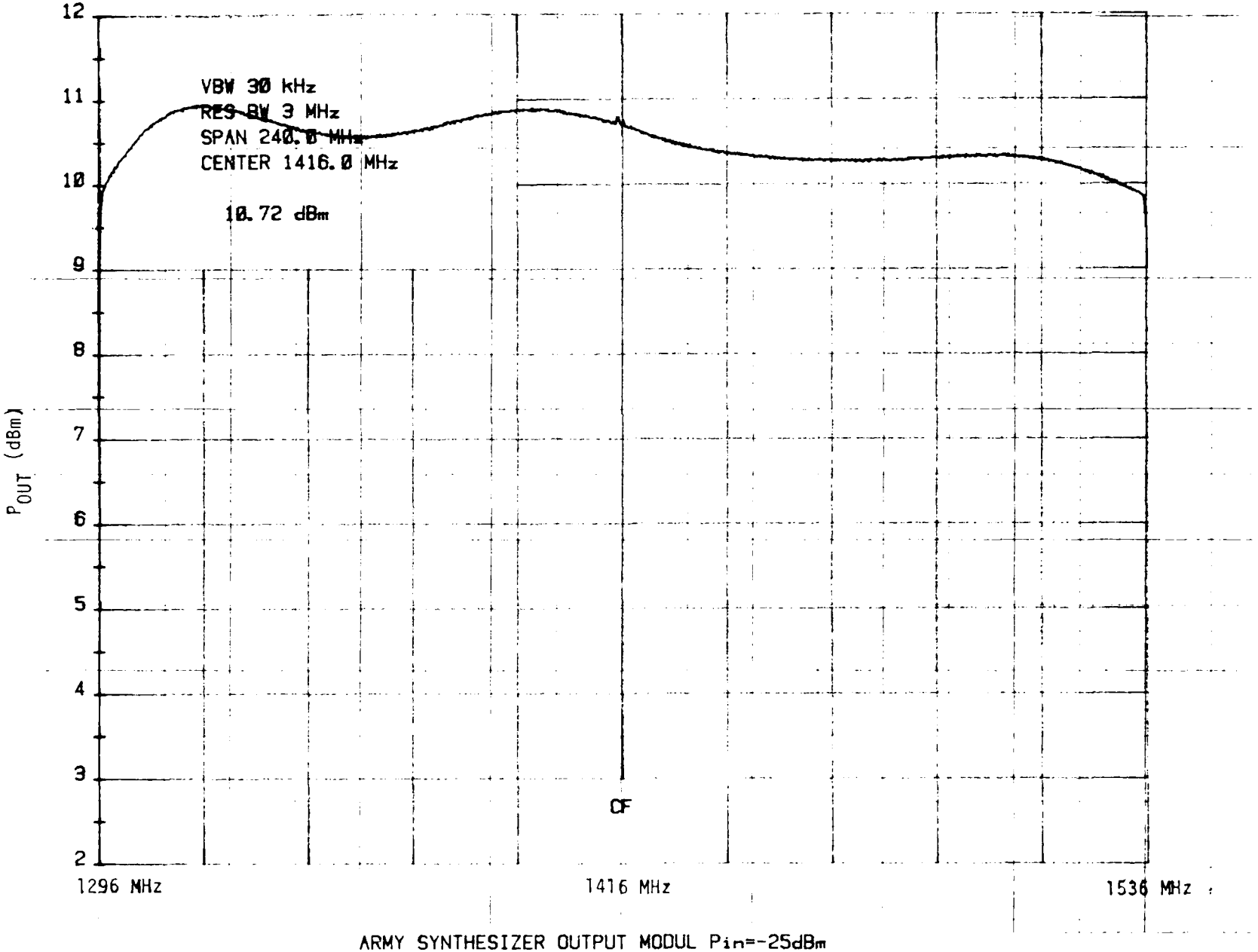
Table 3-10 summarizes the capabilities of the deliverable output module hardware. Figure 3-55 shows the deliverable output module hardware.

3.5.2 Frequency Doubler

As was mentioned above, a frequency doubler is required as part of the output module to double the synthesizer module output frequencies up to the required 1296-1536 MHz operating range. To minimize cost, complexity, and to improve temperature performance, a passive diode doubler design was chosen. A schematic for the circuit is shown in Figure 3-56. Each of the diodes conducts for half a cycle resulting in full wave rectification. The output waveform is therefore rich in second-order harmonics. The 180° relative phase is provided by driving one diode from the center pin of TL_1 while driving the other from the jacket. Both transmission lines also serve as idlers for even-order harmonics and serve to suppress odd-order harmonics. As idlers, the transmission lines provide low impedance paths at the diode inputs for even-order harmonics and high impedance paths at odd-order harmonics.

The performance of the doubler is shown in Figures 3-57 and 3-58 and summarized in Table 3-11. The results indicate worst case spur level as -9 dBc for the third-order harmonic. The design was not optimized for spur rejection since filters following the doubler provide over 70 dB rejection to harmonically related spurs. (Unmatched diodes, an unbalanced power split, and improper phase at the diode inputs all contribute to the presence of harmonically related spurs at the output.) The spur performance for the non-optimized design has been shown to be more than adequate in this circuit application.

Figure 3-52. P_{OUT} vs P_{IN} AT 703 MHz



ARMY SYNTHESIZER OUTPUT MODUL Pin=-25dBm

Figure 3-53. P_{OUT} vs FREQUENCY

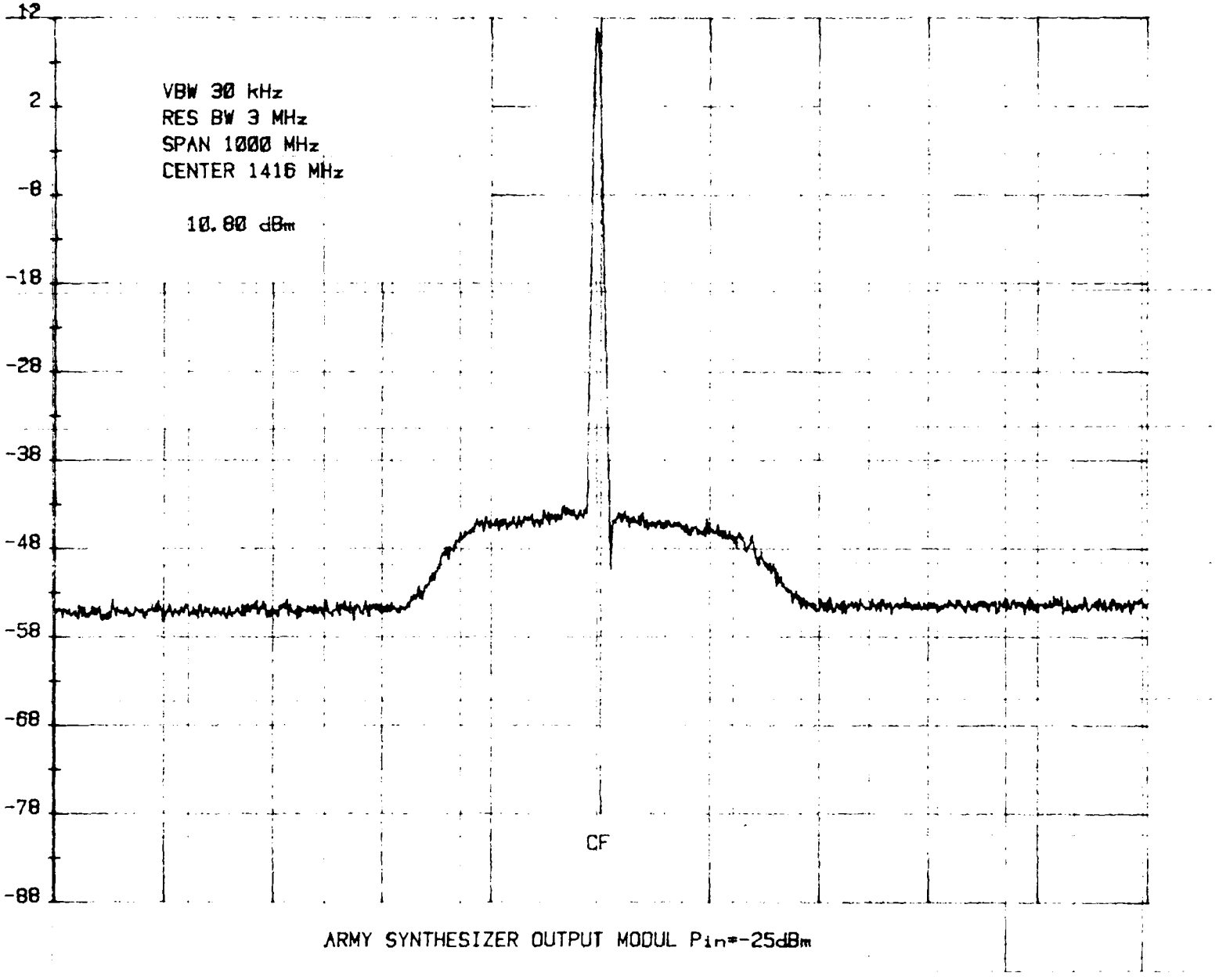


Figure 3-54. OUTPUT MODULE WIDEBAND PERFORMANCE

Table 3-10. FREQUENCY SYNTHESIZER OUTPUT MODULE SPECIFICATIONS (+25°C AMB)

ITEM NO.	PARAMETER DESCRIPTION	REQUIRED PERFORMANCE	CAPABILITY	COMMENTS
1	DC Power	Minimum	2 W	Calculated Power (Breadboard measurement was 3.8 watts).
2	P_{IN} (648 to 768 MHz)	$\geq$ -22 dBm	$\geq$-28 dBm	Breadboard measurement.
3	P_{OUT} (648 to 768 MHz)	+10.0 $\pm$1.0 dBm	+10.3 $\pm$0.5 dBm	Calculated Value (Breadboard measurement was +10 $\pm$0.2 dBm)
4	Frequency Response			
	-1 dB_L Bandwidth	1296 MHz	1280 MHz	Breadboard measurement.
	-1 dB_H Bandwidth	1536 MHz	1600 MHz	Breadboard measurement.
5	VSWR	$\leq$2.0:1	$\leq$1.9:1	Breadboard measurement.
6	Spurious Response	>-70 dBc	>-65 dBc	Breadboard measurement.

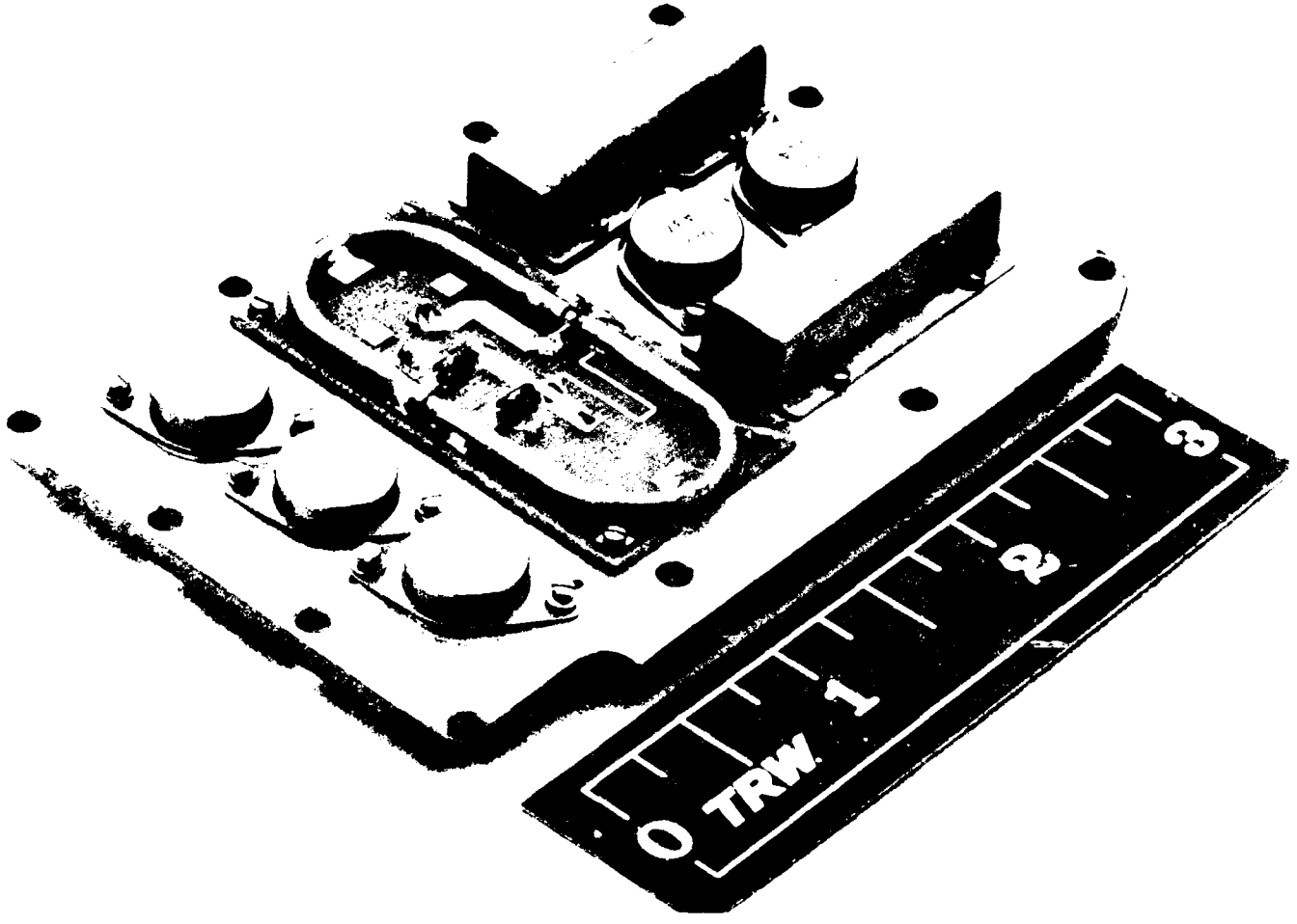


Figure 3-55. OUTPUT MODULE HARDWARE

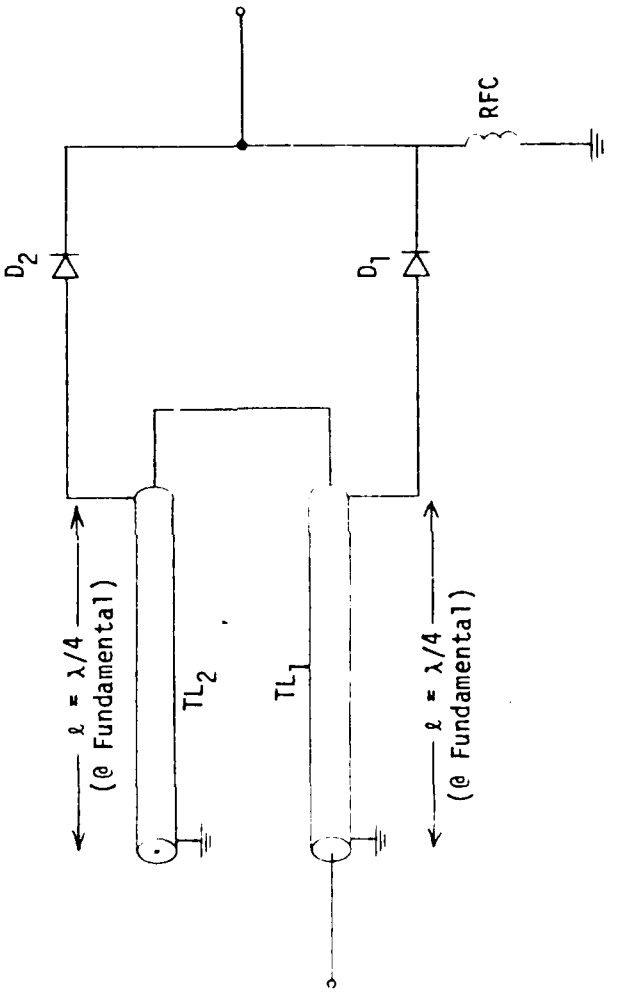


Figure 3-56.

AD-A107 539 TRW DEFENSE AND SPACE SYSTEMS GROUP REDONDO BEACH CA F/G 9/5
SURFACE ACOUSTIC WAVE MICROWAVE OSCILLATOR AND FREQUENCY SYNTHE--ETC(U)
SEP 81 D J DODSON, M Y HUANG, M D BRUNSMAN DAAB07-78-C-2992
DELET-TR-78-2992-F NL

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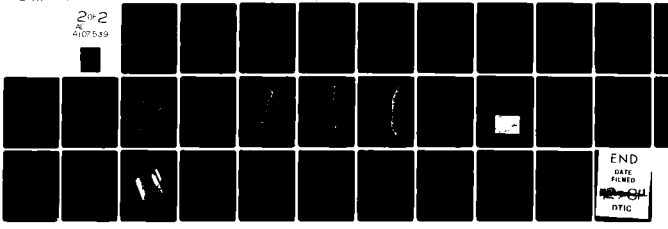


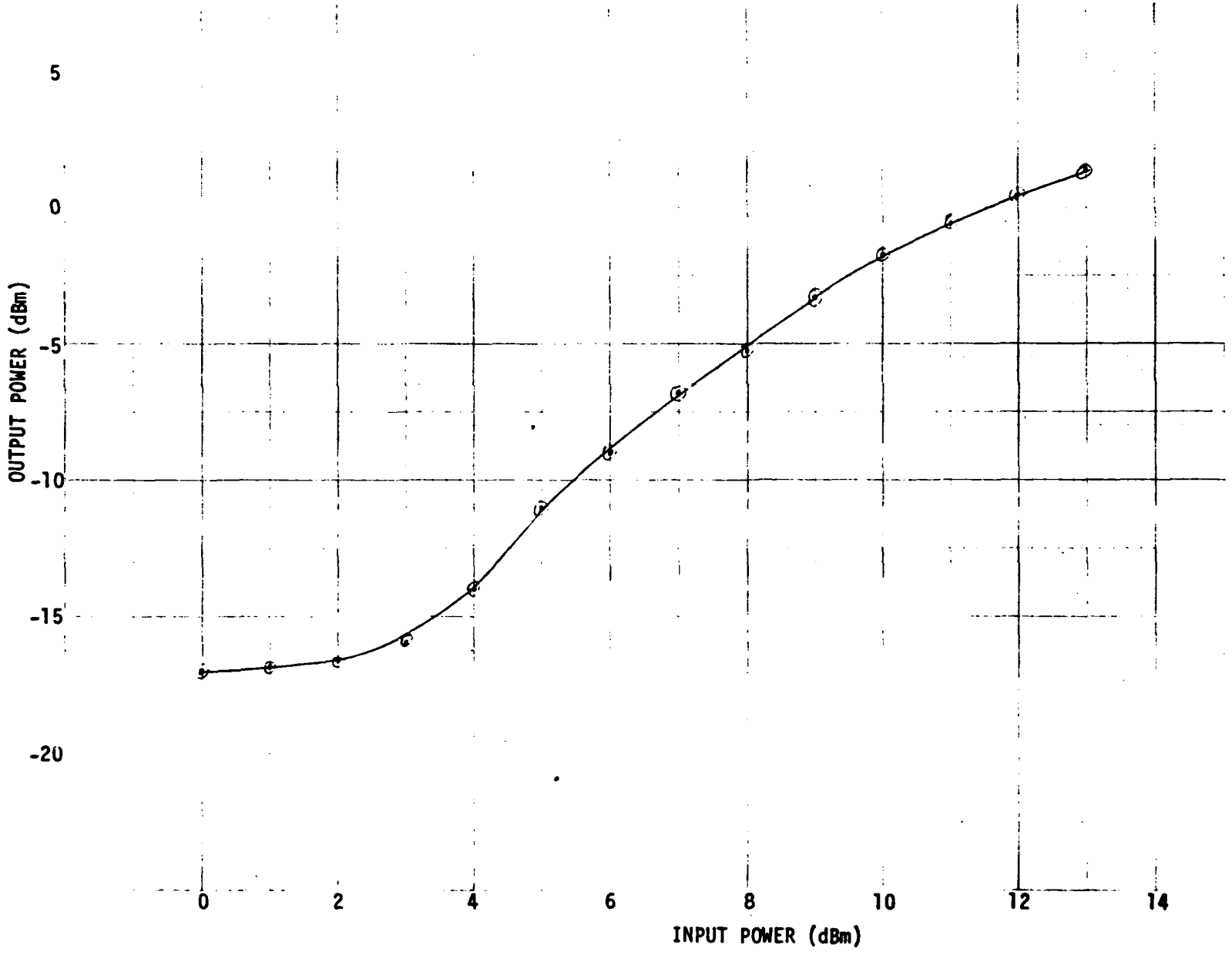


Figure 3-57. FREQUENCY DOUBLER - POWER OUT vs POWER IN

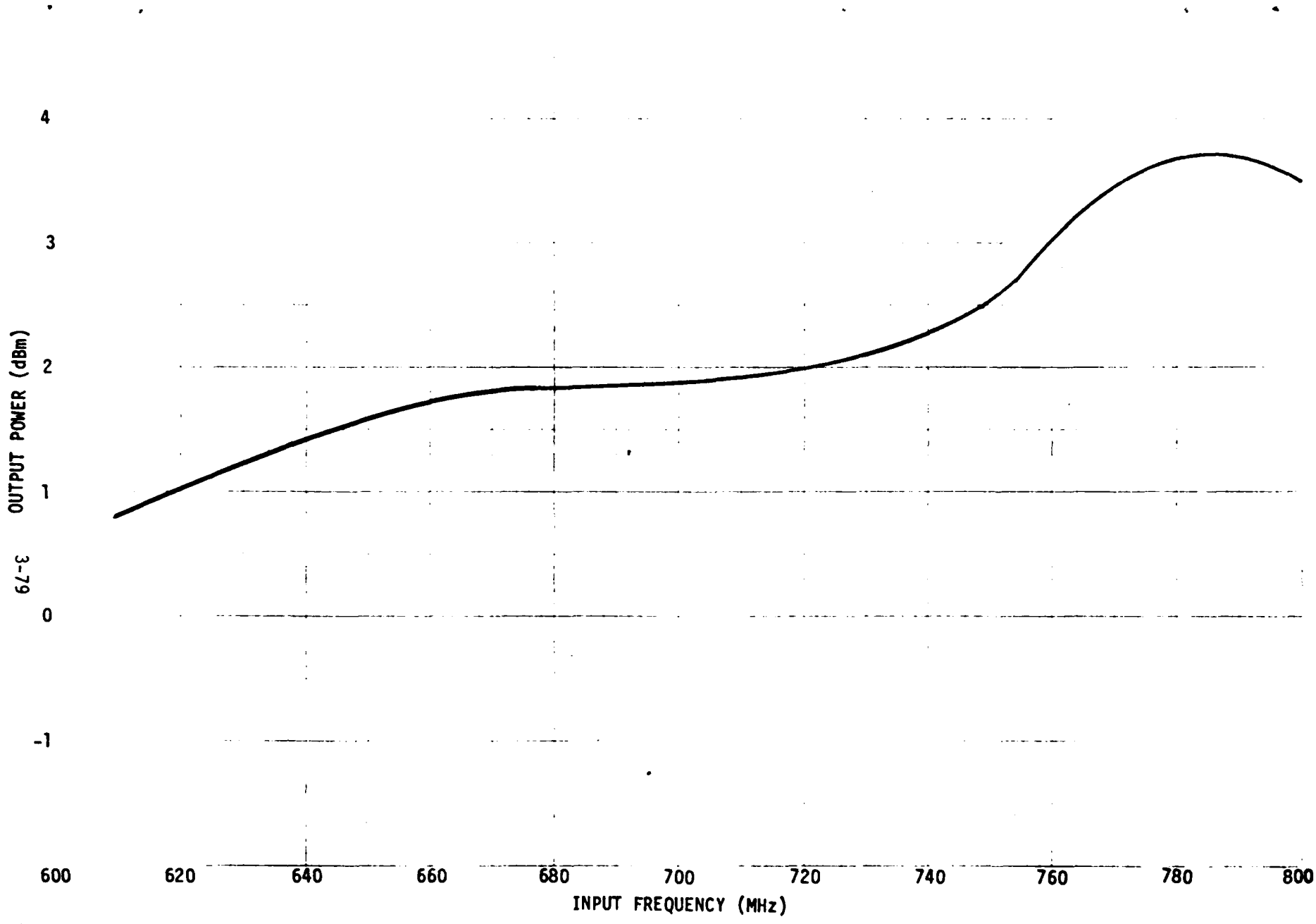


Figure 3-58. FREQUENCY DOUBLER - OUTPUT vs FREQUENCY

Table 3-11. FREQUENCY DOUBLER REQUIREMENTS VS CAPABILITIES SUMMARY

ITEM NO.	PARAMETER DESCRIPTION	REQUIRED PERFORMANCE	CAPABILITY	COMMENTS
1	Input Frequency	648-768 MHz	600-800 MHz	
2	Input Drive Level	$\leq$ +15 dBm	+13 dBm typ.	
3	Conversion Loss	<15 dB	11.5 dB typ.	
4	Harmonic Rejection			
	f_1 (Fundamental)	>0 dBc	$\geq$ -11 dBc	Filters follow the doubler to reduce out-of-band spurs.
	f_2 (Times 3)	>0 dBc	$\geq$ -9 dBc	

4.0 HARDWARE CONSTRUCTION SUMMARY

During the construction phase of the synthesizer, several problem areas encountered with the I.L.O. and synthesizer module/multi-layer board (MLB) hardware were overcome by work-around solutions, which upon unit completion resulted in compromised overall performance. The nature of these hardware problems often required additional circuitry to be implemented supplemental to the already assembled/fabricated unit. Therefore, a tradeoff between achieving functional operation and reduced dynamic performance typically had to be made.

In particular, the spurious output performance of the synthesizer was significantly degraded. The major source of generated in-band spurs present at the synthesizer output are attributable to ADM-1 and package feed-thru, where the unselected mixer input tones appear at the mixer output port anywhere from -30 to -35 dBc. Functional operation of the ADM-1 circuitry was obtained after several circuit re-design efforts were undertaken to adapt the modified ADM configuration, as defined previously in detail. In the final ADM-1 packaging scheme, a Kovar septum was placed between the input amplifier/divider and mixer chips in an attempt to eliminate the direct coupling path from ADM input to output. This effort reduced direct input to output coupling by 10 to 12 dB as measured on a separate ADM chip test fixture.

Had this generation of modified RF-LSI circuitry undergone an additional packaging iteration, similar to the coplanar technique used in obtaining 60 dBc isolation in the SP4T switches, similar -50 dBc spurs would be realized at the ADM outputs.

Other problem areas directly affecting the introduction of spurious tones at the synthesizer output were (a) off-chip lowpass filters at the divider output, (b) off-chip biasing networks at the divider and mixer inputs, and (c) matching networks introduced at the switch input pins of the multi-layer PC board.

4.1 Multi-Layer Board (MLB)

In order to perform the complex mix-and-divide as well as switching functions of the direct synthesizer, a multi-layer processing scheme was employed which utilized the inherent isolation feature of stripline technology. By laying the multi-layer PC board out in such a way that a separate layer of the 10-layer "sandwich" structure was dedicated solely to each of the four primary synthesizer tones, particular attention was given to maximizing isolation at the input ports of the SP3T RF switches. In addition, isolated ground plated-thru holes and ground barriers were utilized where routing of RF lines on adjacent layers appeared in close proximity of one another at feed-thru points to the component layer of the MLB.

Two problem areas associated with the layout of the MLB arose during fabrication of the synthesizer module. Both problems had been researched prior to commital of the layout design by the drafting team assigned to the board as well as the engineering personnel working the isolation aspects of multi-layer design at the frequencies involved. Both problems affected the direct coupling between the four primary synthesizer module tones, in particular, direct coupling between the two center tones (486 and 567 MHz) of the board, and the lack of isolation between the four switch input points on each of the four distinct frequency layers.

The coupling mechanism between the 486 and 567 MHz input tones appeared to be attributable to both a lack of sufficient grounding between the 486 and 567 MHz board layers as well as a proximity or direct coupling effect. An improvement in isolation between the 486 and 567 MHz, as well as to the other board tones, was achieved by placing two ground barriers through the MLB structure, isolating the 486 and 567 MHz input launching points from the other tones throughout the board.

The layout philosophy taken on each of the distinct RF carrying layers of the MLB was one whereby each line segment from the four switch input points (for a given input frequency) was to be constructed of 200 ohm line segments, connected in parallel to present a 50 ohm line impedance, and then routed to their respective launching point at the tone generator input of the MLB. It was theorized that no matching networks would be required between the tone generator output - MLB "50 ohm" interface. Similarly, in addition, no isolation be required between switch input line segments to insure uniform

power distribution among the four switches. The latter assumption proved to result in power level variation, by as great as 12 dB (as measured at the selected switch outputs), and crosstalk problems between adjacent switches operating with multiple applied input tones at comparable power levels.

In order that uniform power levels be applied from the switches to the mixer stage of the ADM-1 circuitry, the result of which would produce a continuously flat swept output spectrum, a scheme of elaborate matching or padding at the switch inputs and/or outputs had to be adopted. No attempt was made at this point to improve tone-to-tone isolation at the switch input ports, only to determine the machanism by which uniform power distribution could be attained at the switch outputs.

Swept frequency return loss measurements made at the switch input ports of an unassembled MLB seemed to indicate that the source of the power variation effect was VSWR mismatch and not an attenuation problem associated with unequal line loss at a particular switch location. Therefore, frequency selective networks (shunt inductors) were applied to the switch inputs (of the assembled MLB) measured at the highest power level in an attempt to route the applied signal field to the lower level input ports. This method was repeated at all switches exhibiting the power balance problem, the result of which yielded signal level variation no greater than 2 dB for any selected switch-input frequency.

4.2 ADM-1 Circuitry

As previously discussed, hardware problems encountered with the ADM-1 circuitry, as fabricated as a single RF-LSI device, required that certain chip filtering, biasing, and level setting functions be provided at the "off-chip" level. Satisfactory functional operation of the conglomerate circuitry provided the amplify-divide-mix operation as proposed, but fell short of required spurious performance, generally due to the nature of the solution employed in interconnecting the discrete device chips in a single 24-pin flat package.

Due to the digital technology employed in the programmable divider circuitry, even and odd ordered harmonics are produced as high as -15 dBc at the divider output. Off-chip lowpass filters were designed to provide stopband attenuation in excess of -50 dBc. The transition bandwidth specification for the LPFs was fixed by the need to remove the second harmonic of the divider, in the ÷3 mode, in order to prevent $F_{RF} - 2F_{LO}/3$ spur generation at the mixer output of the first three ADMs. A 7th order Chebychev filter design was easily implemented to fulfill the passband and transition band requirements as mentioned; however, the physical size constraint imposed on the filter layout prevented adequate ground integrity throughout. As a result, degraded high frequency performance was obtained where 3rd and higher order divider output harmonics were present at the LO port of the mixer, capable of mixing as in-band spurs present at levels on the order of -40 dBc, in the first three ADMs.

In order to apply the required DC bias voltages to the input circuitry of the programmable divider and mixer, balanced bridge networks were designed with inductive coupling to prevent the RF signals at the device inputs from modulating the common DC supplies.

The balanced bridge network structure was employed particularly to facilitate offsetting the 1% film resistor arms at the input stage of the mixer. This ability would serve to enable the reduction of even-ordered mixer spurs generated in a doubly-balanced design of the type employed in the ADM circuitry. However, the magnitude of mixer-imbalance produced even-order spurs, by comparison with the spur levels encountered which were attributable to other means, did not require exercising the trimming capability of the balancing networks.

4.3 Commercial Bandpass Filters

Commercially available bandpass filters were designed to filter the IF output of ADM-1 mixers. The filters were designed with two distinct passband frequency ranges to accomodate the difference mode IF and sum mode operation of the #1-#3 and final ADM, respectively. The bandpass of the filter utilized with the low side ADM output frequency range is centered at 425 MHz with a 3 dB bandwidth of 165 MHz. The center frequency of the bandpass filter at the synthesizer output is 708 MHz, with the same 165 MHz 3 dB bandwidth.

Figures 4-1 and 4-2 show typical data measured to define the filter 3 dB bandwidth for the filter with f_0 = 425 MHz, and out-of-band performance, respectively. From Figure 4-1 note that the filter insertion loss is measured to be 1 dB at f_0 and the -3 dB points aremeasured at 351 MHz and 510.6 MHz, thereby indicating a 3 dB bandwidth of approximately 160 MHz. From the data measured showing the out-of-band attenuation characteristics of the filter in Figure 4-2, it can be seen that harmonic products mixed by the ADM mixer/A2 circuitry which fall on the low IF side of the filter curve will not be attenuated as greatly as those on the upper side of the filter. Since this filter is used in an application where the filtered IF bandwidth is generated by a downconversion process, spurious tones present at the low side of the filter passband are more likely to re-mix in successive ADM circuitry than are the high side tones. The relative difference in stopband performance can be seen by imposing the filter's high side transition band slope to the low end of the filter curve of Figure 4-2. From this comparison, the net lack of low-end attenuation is given by:

Stopband Frequency (MHz)	Measured Attenuation (dB)	Translated Attenuation (dB)	Net Attenuation Increase (dB)
320	-18.0	-22	+4
310	-22.5	-32	+9.5
300	-27.0	-42	+15
290	-30.0	-52	+22
250	-39.0	-52	+13

Again, as a result of the poor low-side stopband performance indicated in Figure 4-2, divider harmonics present at the first mixer LO input port are more likely to mix and appear in successive ADM RFCS-1 input spectra. This condition becomes worse at the input to the #4 ADM circuitry, by virtue of the compounding effect resulting from three stages of similar filtering inadequacy.

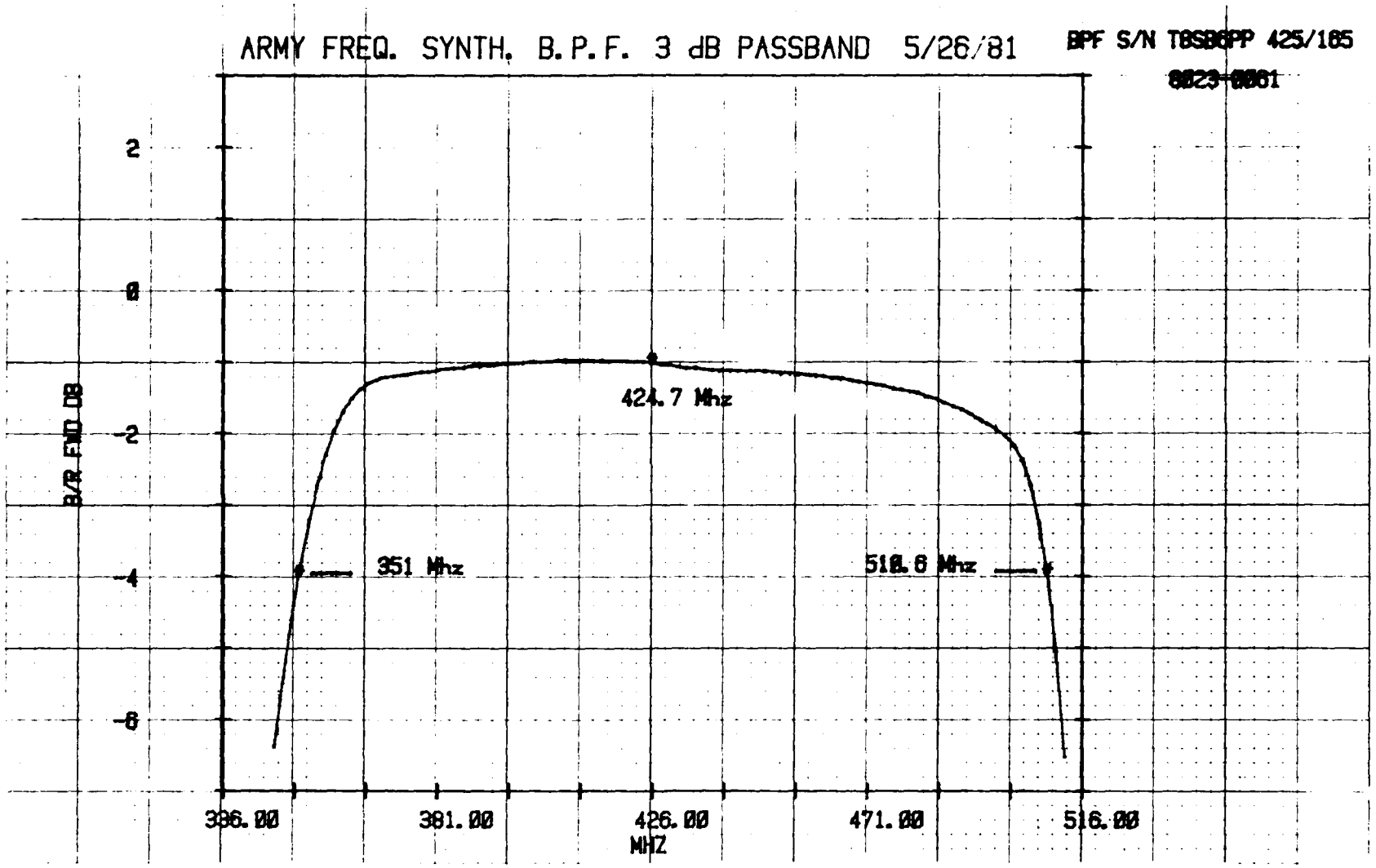


Figure 4-1. BANDPASS FILTER, 3 dB PASSBAND DATA

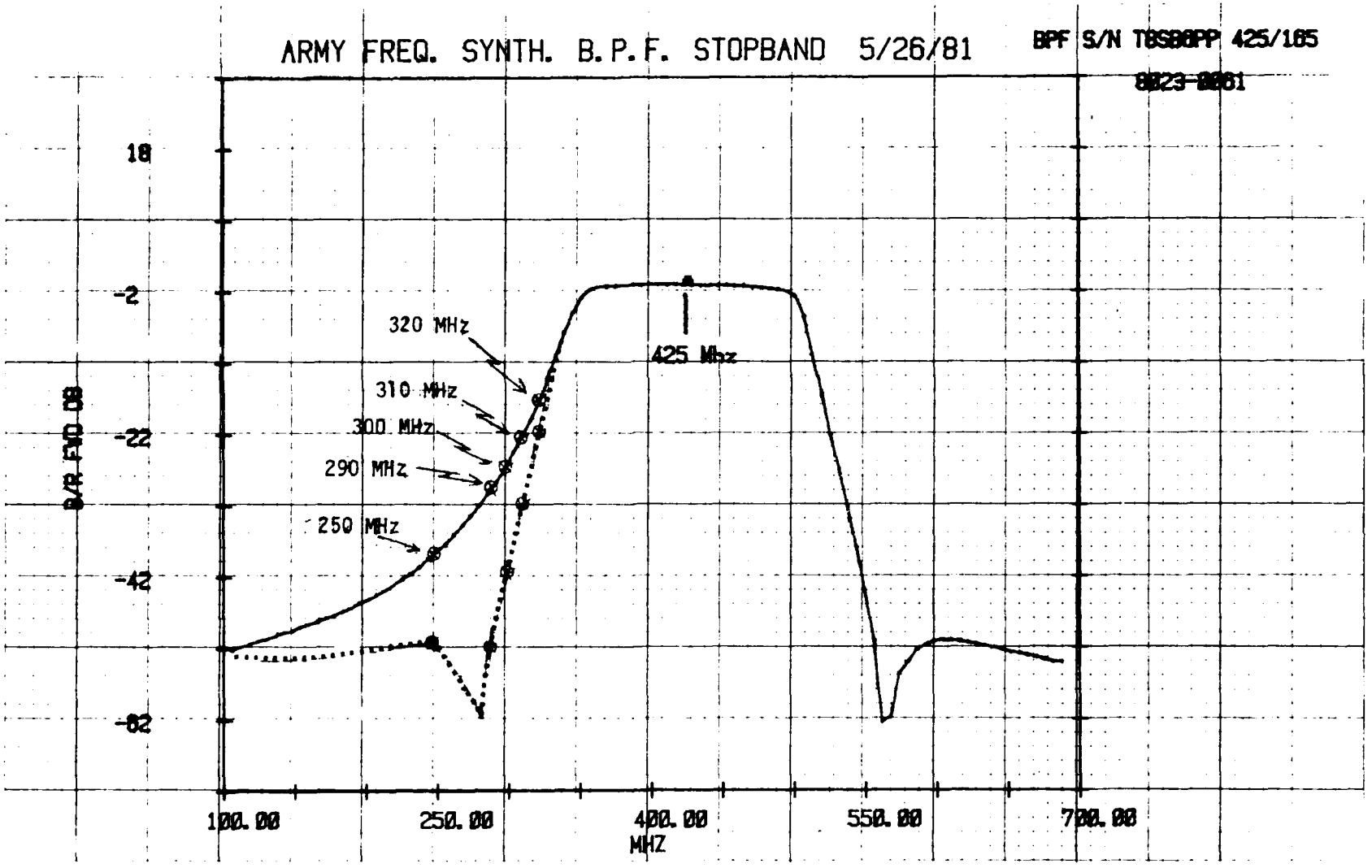


Figure 4-2. BANDPASS FILTER OUT-OF-BAND DATA

5.0 HARDWARE TEST RESULTS

The design parameters and performance of individual modules comprising the synthesizer subsystems have been described in detail in previous text. Subsequent data presented was obtained during evaluating the performance of the integrated synthesizer, and a comparison of measured capabilities is made against the proposed system requirements.

5.1 Frequency Accuracy

Figure 5-1 shows the synthesizer output at selected discrete frequencies ranging from 1326 to 1356 MHz in 3 MHz increments. The control box was interfaced in the single frequency mode to step the synthesizer through a 30 MHz range. The data was taken on the Hewlett-Packard 8568A spectrum analyzer in the storage max-hold mode. Note that the frequency counter option of the 8568A was utilized to measure a frequency spacing accuracy of 3.00 MHz. Figures 5-2 and 5-3 similarly highlight the frequency spacing accuracy of the frequency syntehsizer, with controller in the single frequency mode. Again, the HP 8568A spectrum analyzer was used in obtaining the data as given.

5.2 Synthesizer Module Swept Output

Figure 5-4 is a plot of the synthesizer module output spectrum, prior to output module, with the control box interfaced in the sweep mode. The full frequency capability of the synthesizer is measured again with the HP 8568A spectrum analyzer, as is shown by the swept output spectrum from 648 to 768 MHz. Note that the total variation in synthesizer module output power is approximately 5 dB. Three distinct regions in the output spectrum are seen as the last ADM in the synthesizer module chain selects each of the three primary tones at its mixer RF port input. The 567 MHz input being lower in power than the other three tones, therefore provides a lower IF signal level over the bandwidth for a given mixer LO drive level.

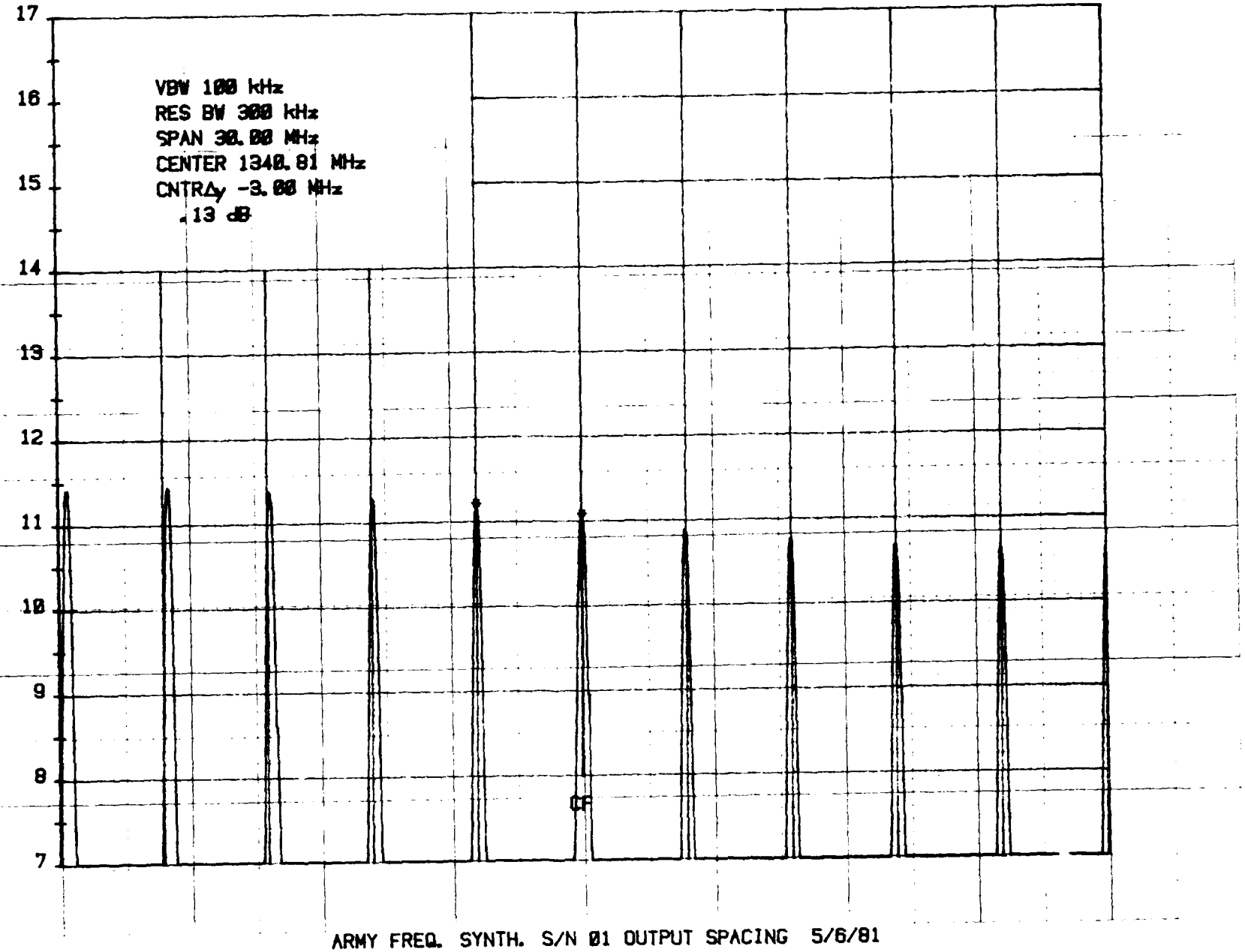
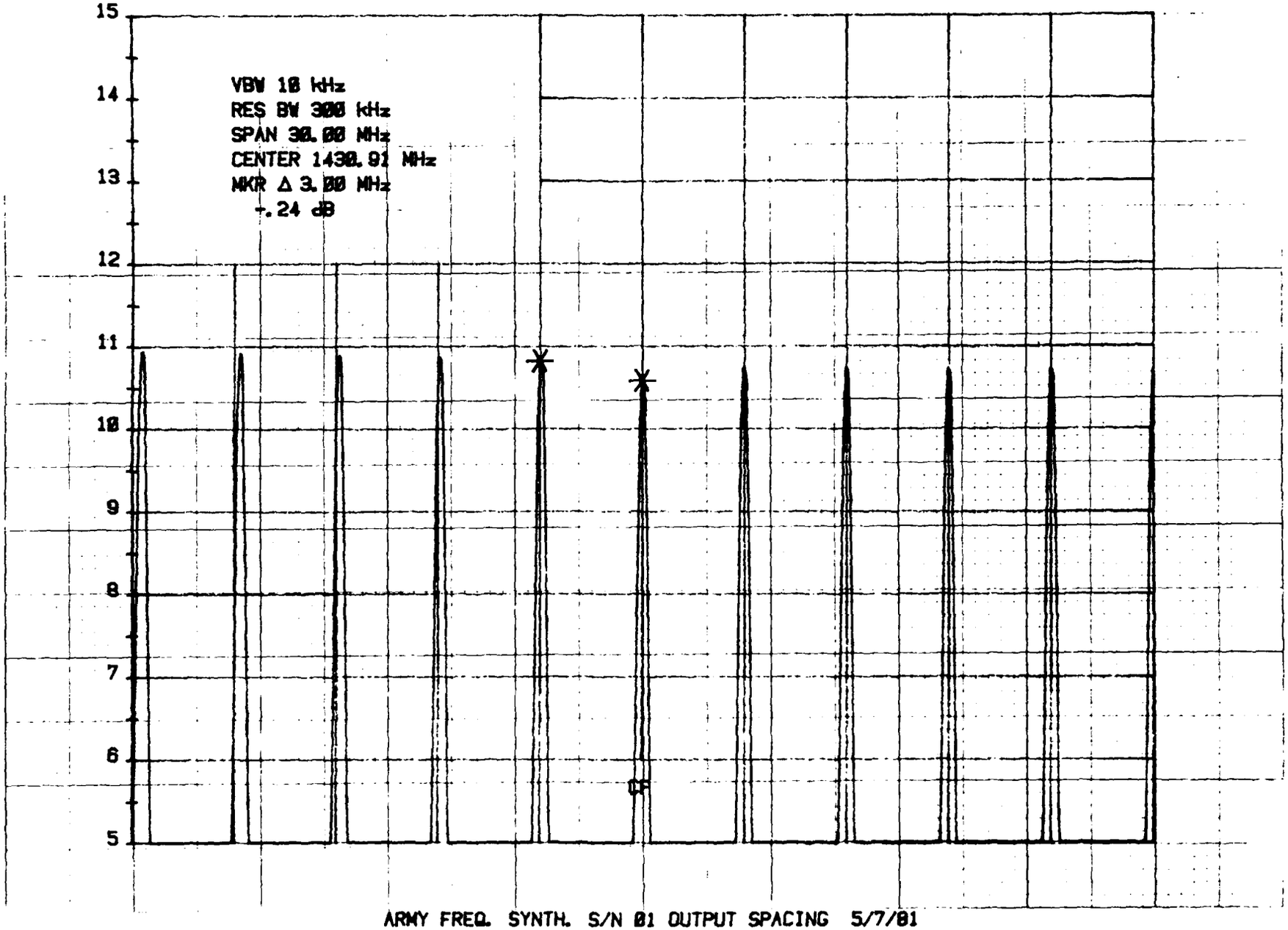


Figure 5-1. OUTPUT TONE SPACINGS, 1326 to 1356 MHz, 3 MHz STEPS



ARMY FREQ. SYNTH. S/N 01 OUTPUT SPACING 5/7/01

Figure 5-2. OUTPUT TONE SPACINGS, 1416 to 1446 MHz, 3 MHz STEPS

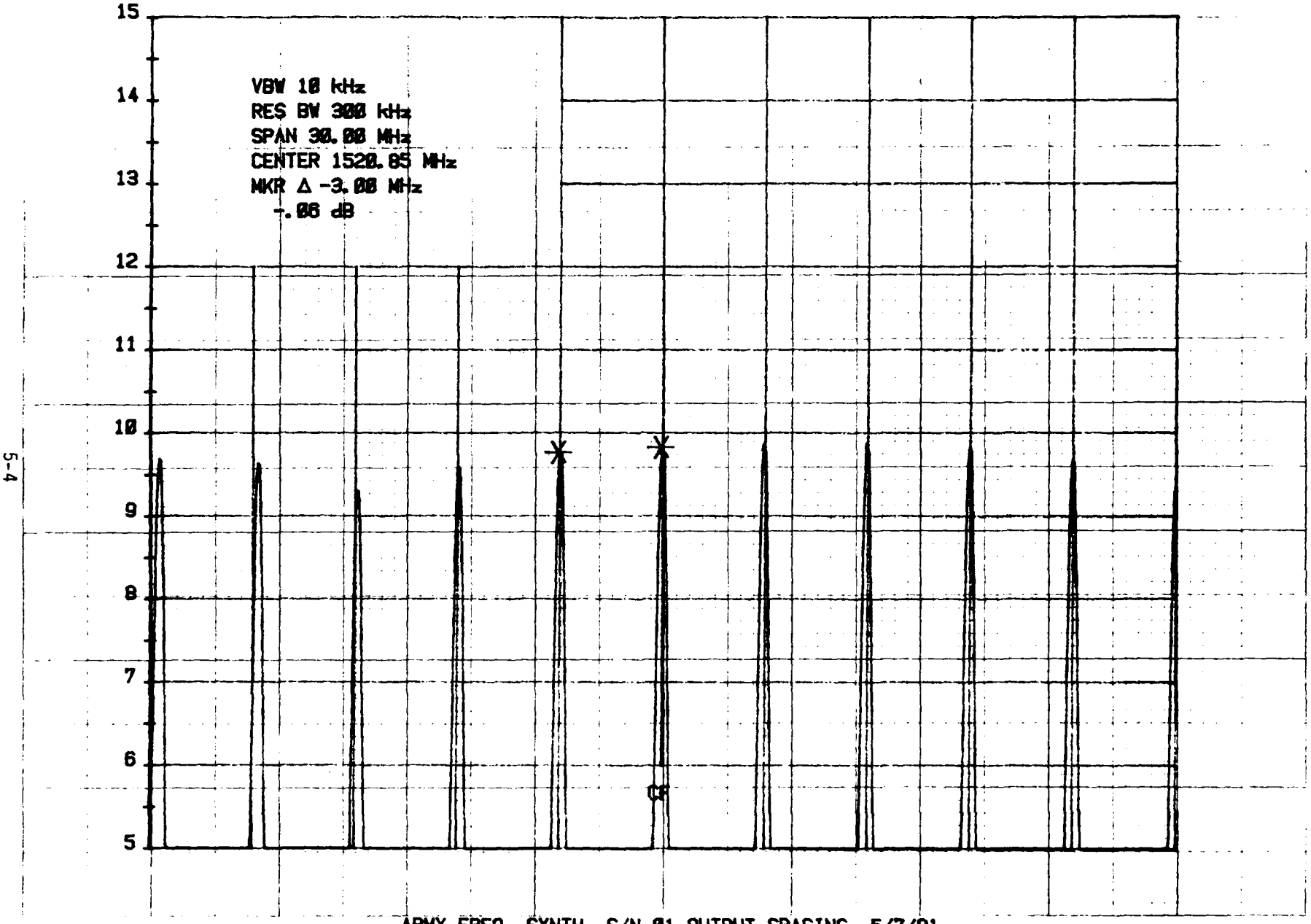


Figure 5-3. OUTPUT TONE SPACINGS, 1506 to 1536 MHz, 3 MHz STEPS

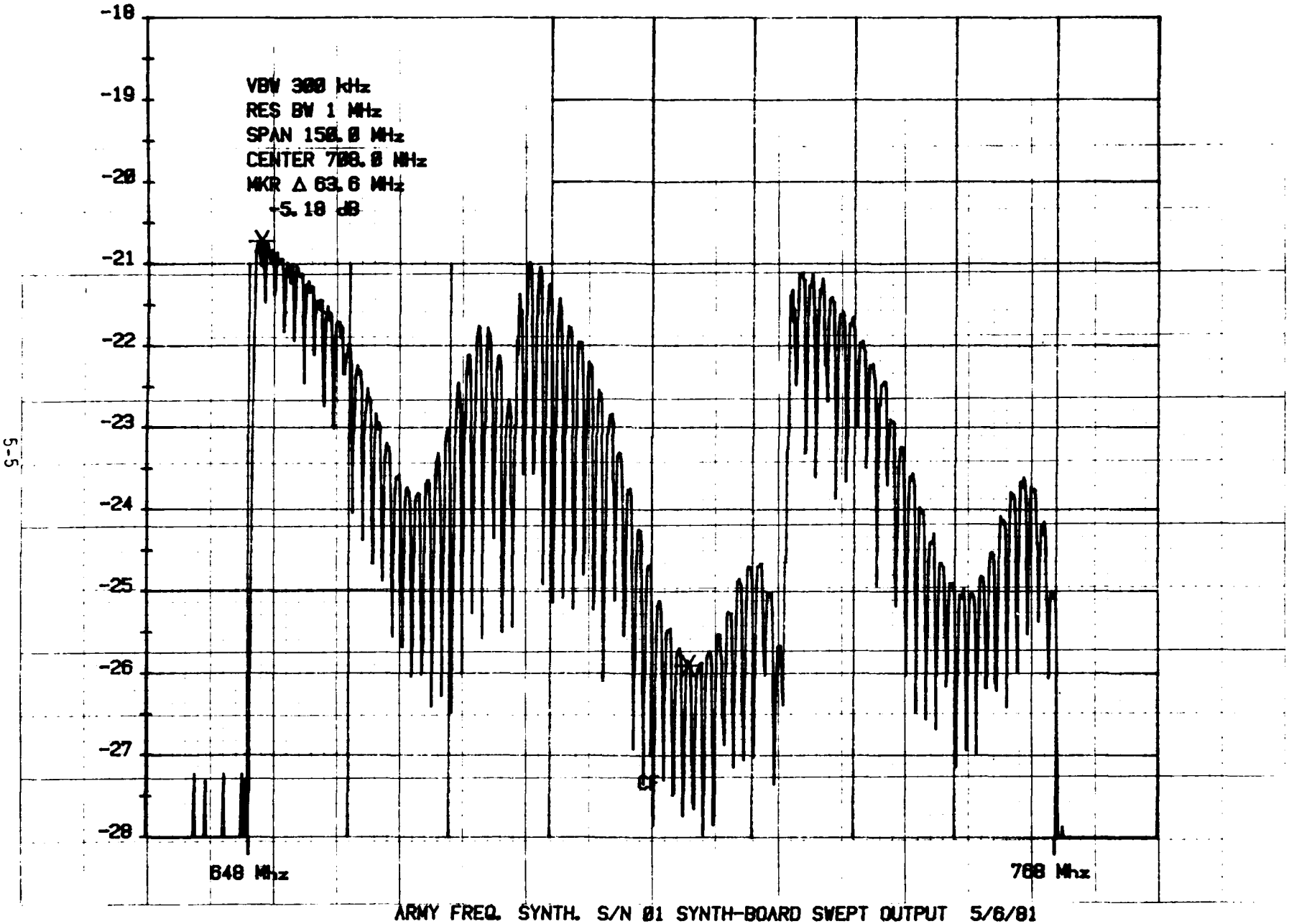


Figure 5-4. FREQUENCY SYNTHESIZER SWEPT OUTPUT SPECTRUM, SYNTHESIZER BOARD OUTPUT

5.3 Synthesizer Swept Output

Figure 5-5 is a plot of the final synthesizer swept output spectrum under the drive conditions presented by Figure 5-4. Notice that the minimum drive level presented at the synthesizer module output at 712 MHz is sufficient to saturate the gain stages of the output module, resulting in a swept output spectrum well within a measured 10 $\pm$1.3 dB range. Also note that the total output power variation over frequency is approximately 2.6 dB.

5.4 Synthesizer Module Single Output Spectrum

Figure 5-6 is a plot of the stationary spectrum at the synthesizer module output with the output selected to be 672.0 MHz. Notice that in a 200 MHz frequency span that a spurious tone is observed to be approximately -40 dBc, with typical spurious levels to be approximately -50 dBc.

5.5 Synthesizer Single Output Spectrum

Figure 5-7 is again a plot of the stationary synthesizer spectrum. This data, taken in a 250 MHz frequency span, shows the synthesizer output at 1415 MHz with in-band spurious tones 15 MHz from the carrier at -30 dBc. Note the general bandpass shape to the spectrum noise floor as a result of the bandpass filters of the output module.

5.6 Switching Speed Data

In order to accurately evaluate the rate at which the synthesizer was capable of producing two distinct output frequencies, independent of output frequency spacing, the test configuration of Figure 5-8 was constructed. Briefly, the test is a measure of the hopping capability of the synthesizer, and is accomplished by comparing the output of the synthesizer to two signal sources, the frequencies of which are identical to those hopped between by the synthesizer under test.

The synthesizer under test's reference input is applied externally to the two reference sources to establish phase coherency. A square wave generator with variable DC offset capability is used to apply the hop command to the UUT. A DC level of greater than 1.5 VDC is required of the square wave "high" amplitude to properly sequence the SP4T of the synthesizer. By applying this trigger word simultaneously to the 2^7 bit of the synthesizer and the horizontal trigger input of an oscilloscope, accurately triggered timing information can be obtained.

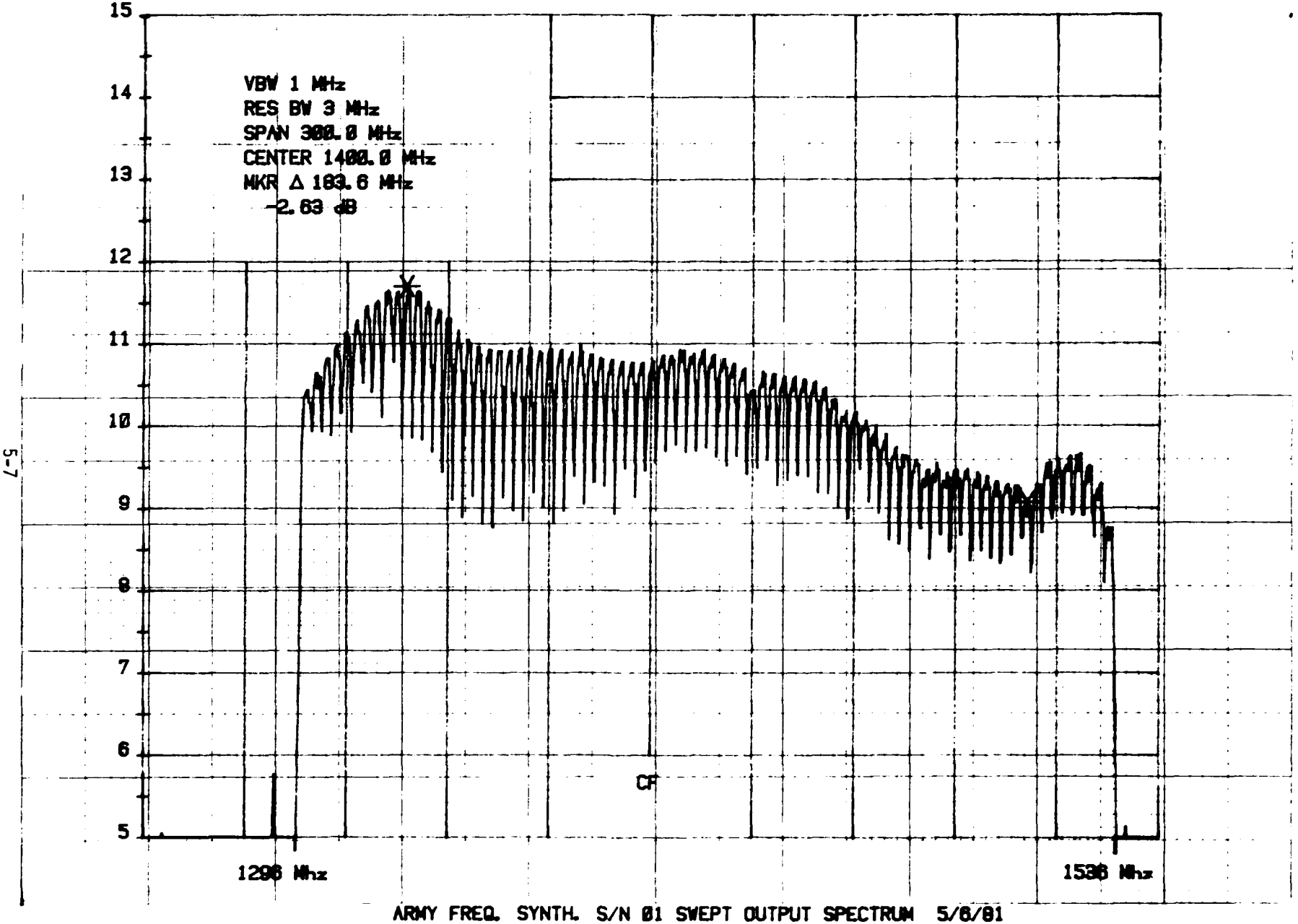


Figure 5-5. FREQUENCY SYNTHESIZER SWEPT OUTPUT SPECTRUM

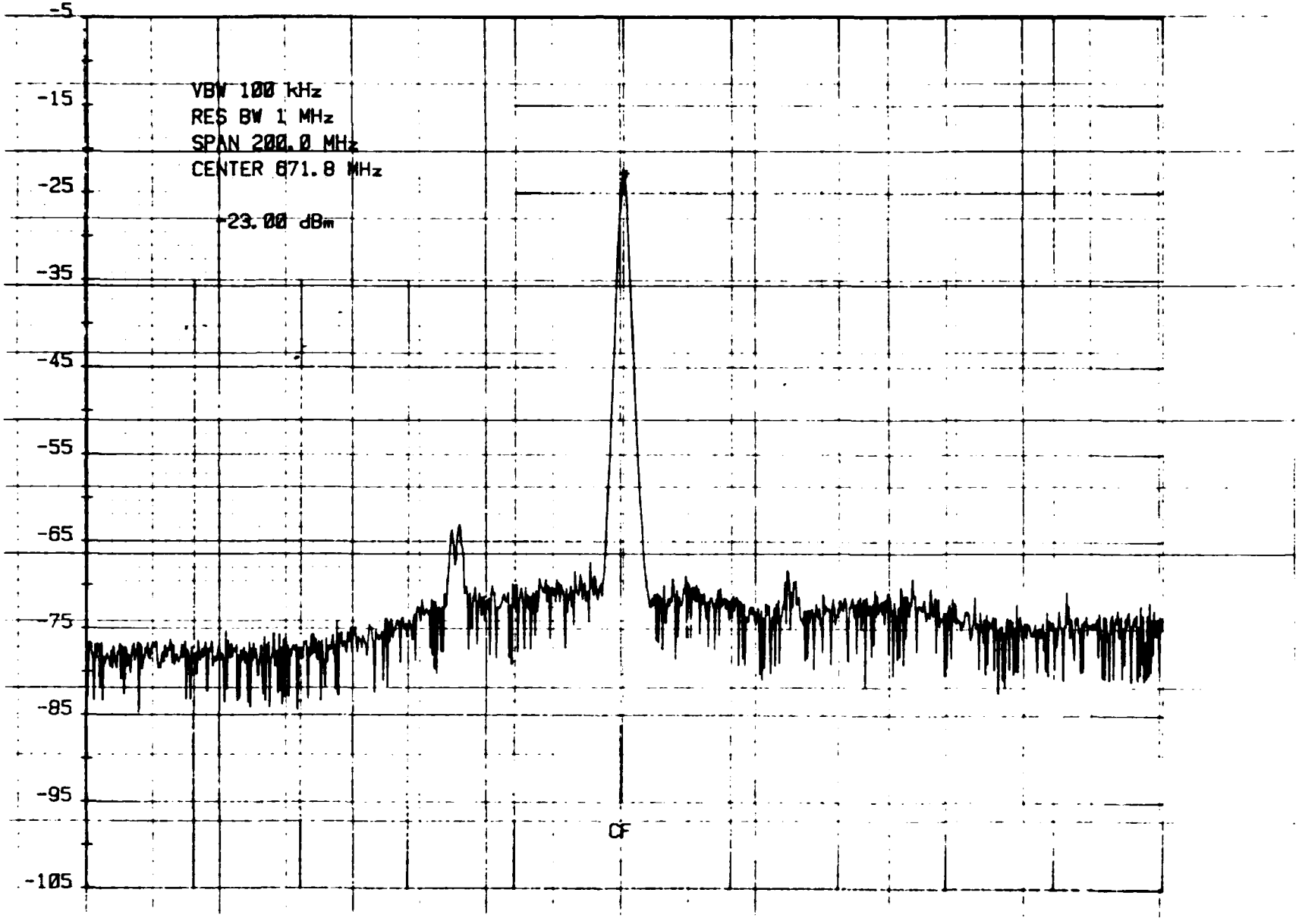


Figure 5-6. FREQUENCY SYNTHESIZER BOARD OUTPUT SPECTRUM 672 MHz SELECTED OUTPUT

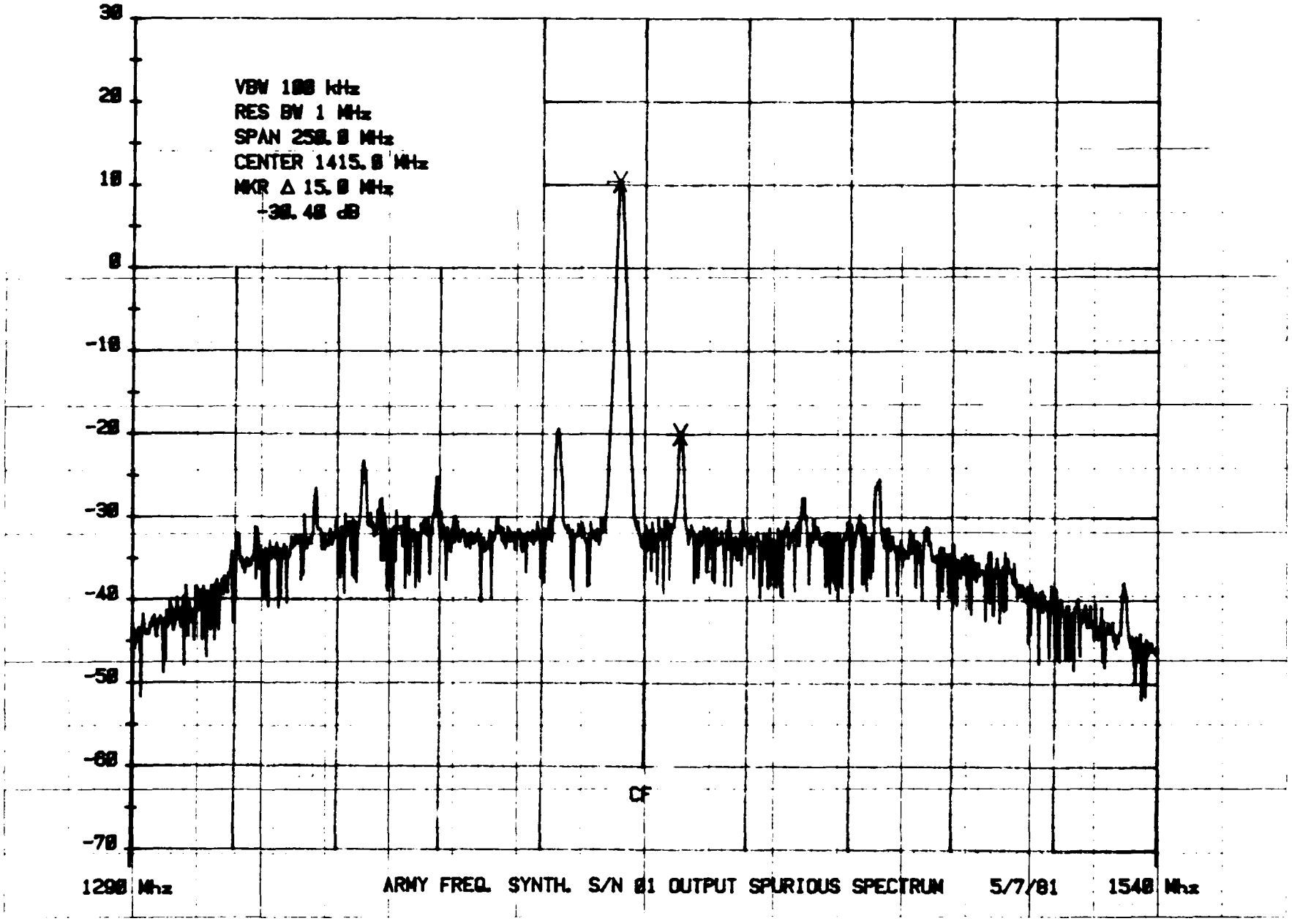


Figure 5-7. FREQUENCY SYNTHESIZER OUTPUT SPECTRUM, 1415 MHz SELECTED OUTPUT WORD

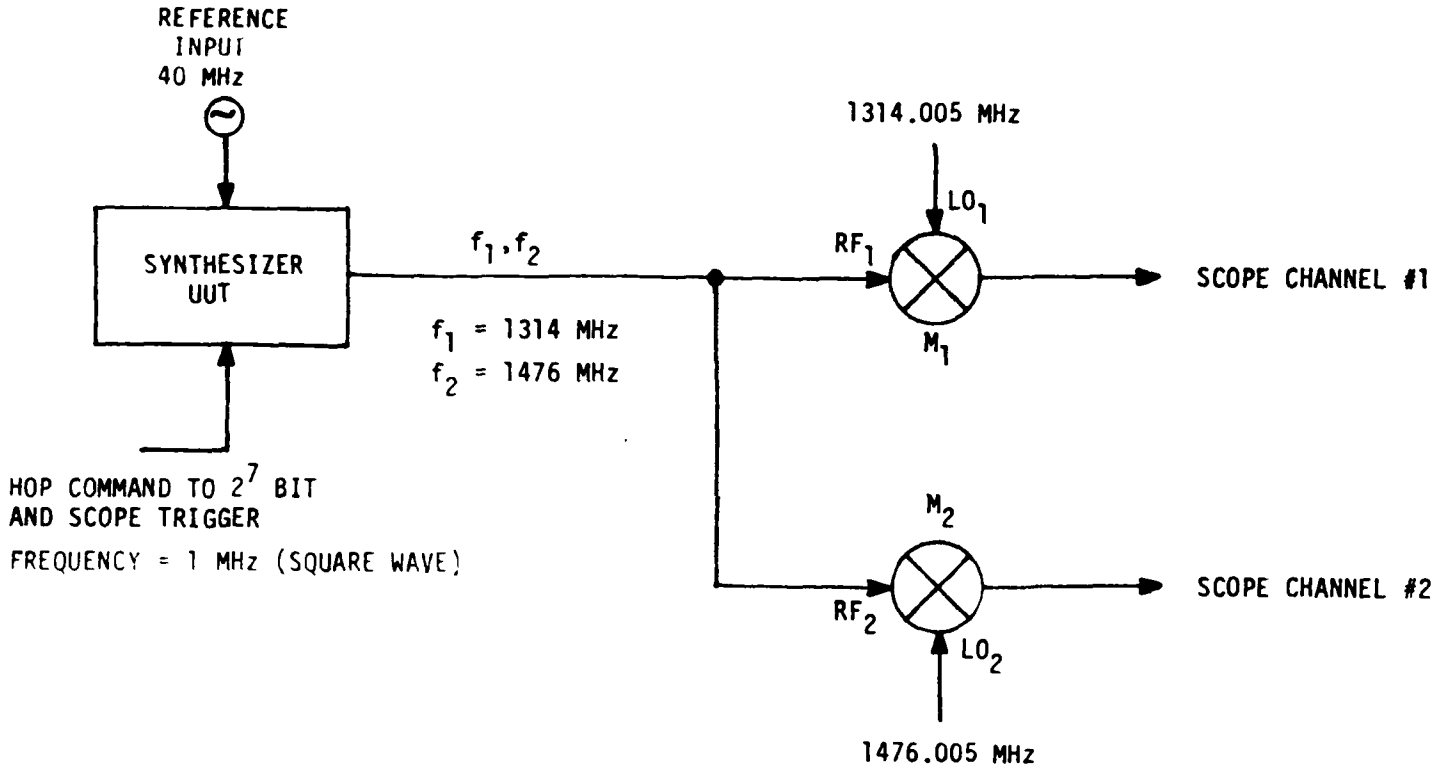


Figure 5-8. SWITCHING SPEED TEST SET-UP

Two commercially available high-level mixers were used to perform the downconversion process. However, two lower level mixers would work as adequately with some attenuation applied to the RF port input levels. The two reference sources are initially offset from the hop frequencies by 5 KHz in order to dramatically define the transition between a difference frequency of 5 KHz and the difference between the reference source center frequencies, as seen at the mixer IF ports. It should be noted that the oscilloscope used to measure the hop rate given in this example was limited to viewing signals in the 100 MHz region. Therefore, a 20 MHz bandwidth limiter was employed to suppress the high frequency portion of the mixer output waveform. For this reason, the solid line portion shown in the accompanying photographs is actually the difference frequency between the RF sources, and is in the range of 150 MHz.

Figure 5-9 is a photograph of the mixer output waveforms. The bottom waveform is the square wave trigger word. Note that when the trigger waveform is "low" the synthesizer is at the lowest output frequency, and vice versa. From Figure 5-9 it can be seen that it takes approximately 60 ns for the synthesizer to react to the command word transition, and the completed act of generating the frequency hop transition takes approximately 20-50 ns with some question as to frequency certainty once the hop has been initiated.

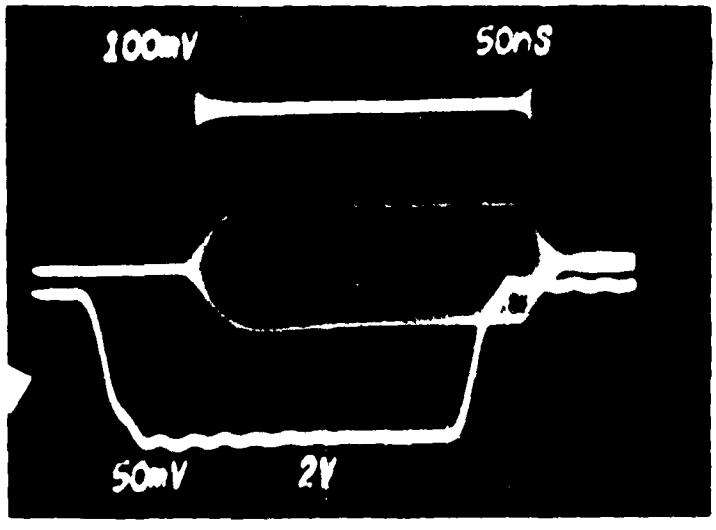


Figure 5-9. MIXER OUTPUT WAVEFORMS

5.7 Phase Noise Data

Figures 5-10 and 5-11 present the spectral phase noise characteristics of the completed synthesizer as measured by the TRW Metrology Department. The single oscillator technique was employed to obtain data for synthesizer operation at center frequencies of 1308 and 1503 MHz. Note that in both cases the synthesizer phase noise was measured to be below 90 dBc at 10 KHz, and is below 110 dBc at 2 MHz.

5.8 Comparison of Capabilities vs Requirements

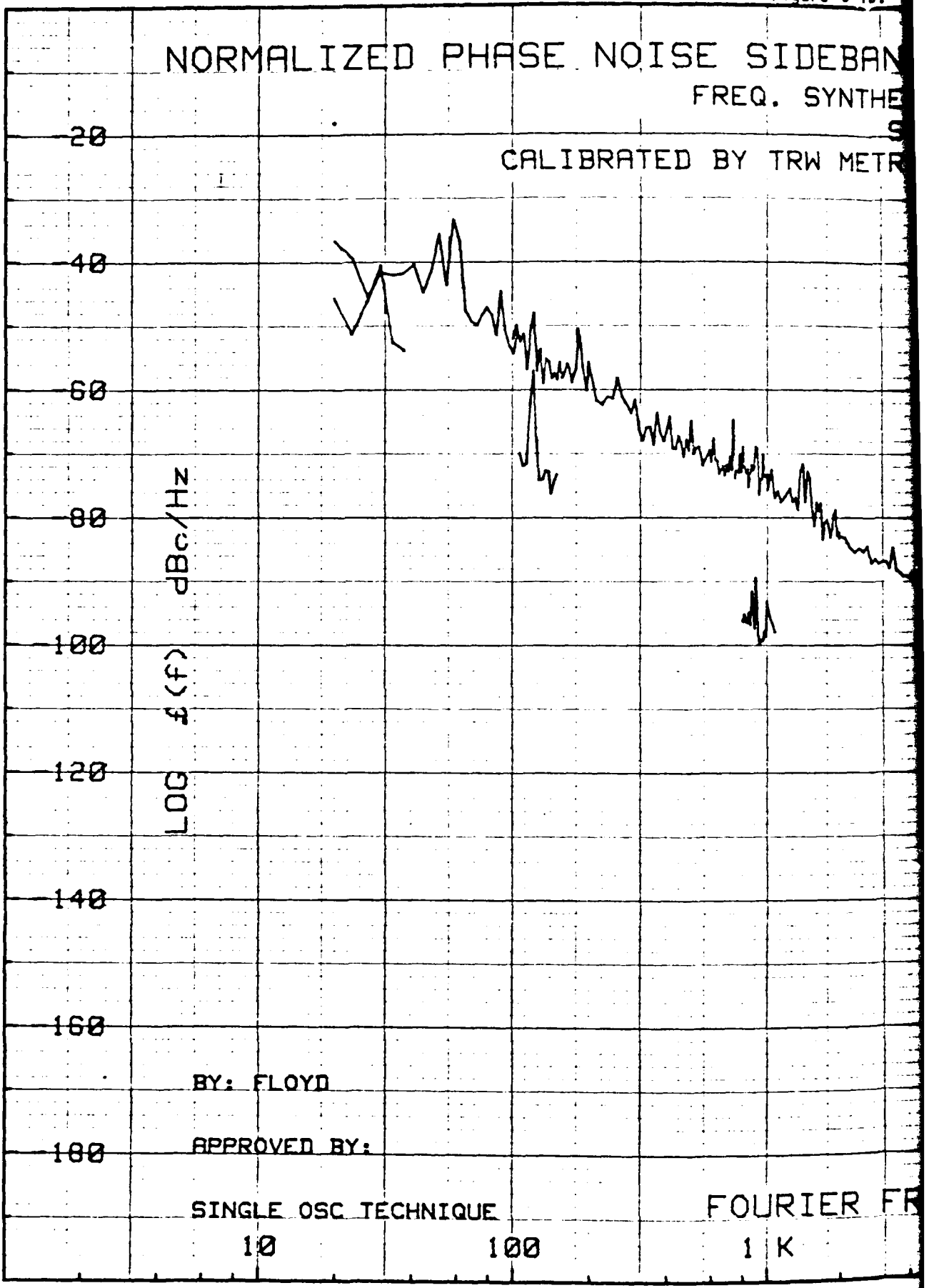
Table 5-1 gives a detailed comparison of measured synthesizer performance to the requirements outlined under the Task II technical requirements section of the contract statement of work.

The packaging configuration utilized for the final synthesizer deliverable unit is given in Figure 5-12. A photograph of the deliverable synthesizer configuration is shown in Figure 5-13.

Table 5-1. FAST HOPPING FREQUENCY SYNTHESIZER FUNCTIONAL REQUIREMENTS vs CAPABILITIES

ITEM	REQUIREMENT	MEASURED PERFORMANCE
Total DC Input Power	≤5.0 watts	17.5 watts
Power Output Per Channel	+10.0 ±1.0 dBm	+10.3 ±1.3 dBm
Switching Speed	Among 51 JTIDS Tones ≤ 1 μs	≤25 ns
Settling Time	<100 ns to within 5.73°	≤ 75 ns
Spurious Response Suppression	≥ 68 dBc	LO feedthru ≥ 30 dBc Other spurious ≥ 43 dBc
Phase Noise	-65 dBc/Hz out to 100 KHz; -80 dBc/Hz out to 1 KHz; >-120 dBc/Hz noise floor	≤-105 dBc/Hz to 200 KHz; -(85 dB - 25 dB/decade) from 200 KHz to 2 MHz
Output Frequency Range	Suitable for use in a terminal that transmits frequencies from 950-1202 MHz	1296.00 to 1536.00 MHz
Number of Frequencies	85	81
Output Frequency Spacing	3.00 MHz	3.00 MHz
Size	≤ 10 in^3	48 $in.^3$ (8" x 6" x 1")

Figure 5-10.


NORMALIZED PHASE NOISE SIDEBAN
FREQ. SYNTHE
S
CALIBRATED BY TRW METR
-20
-40
-60
-80
-100
-120
-140
-160
-180
LOG £(f) dBc/Hz
BY: FLOYD
APPROVED BY:
SINGLE OSC TECHNIQUE
FOURIER FR
10
100
1 K

igure 5-10.

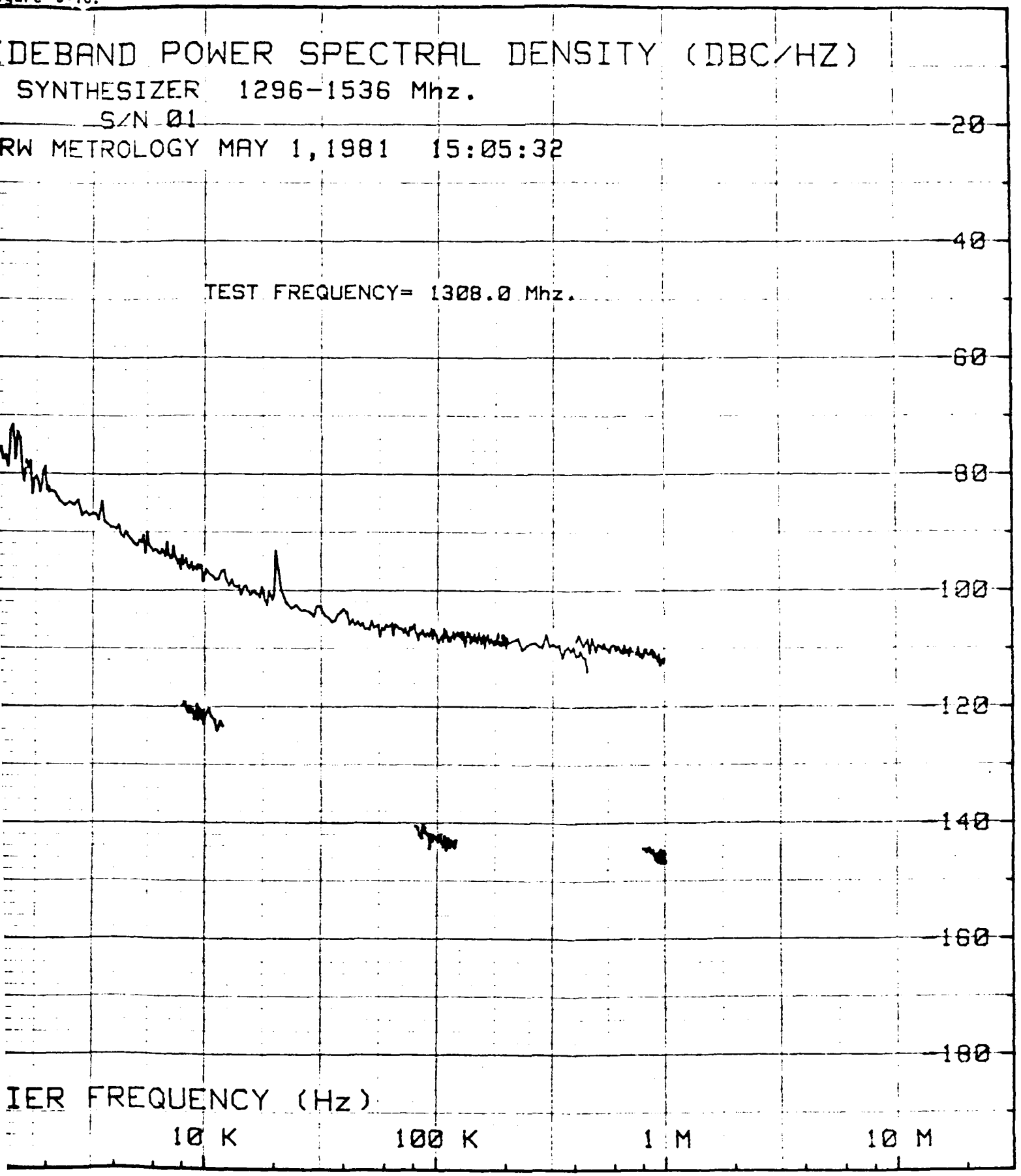

IDEBAND POWER SPECTRAL DENSITY (DBC/HZ)
SYNTHESIZER 1296-1536 Mhz.
S/N 01
RW METROLOGY MAY 1,1981 15:05:32
TEST FREQUENCY= 1308.0 Mhz.
20
40
60
80
100
120
140
160
180
IER FREQUENCY (Hz)
10 K
100 K
1 M
10 M

Figure 5-11.

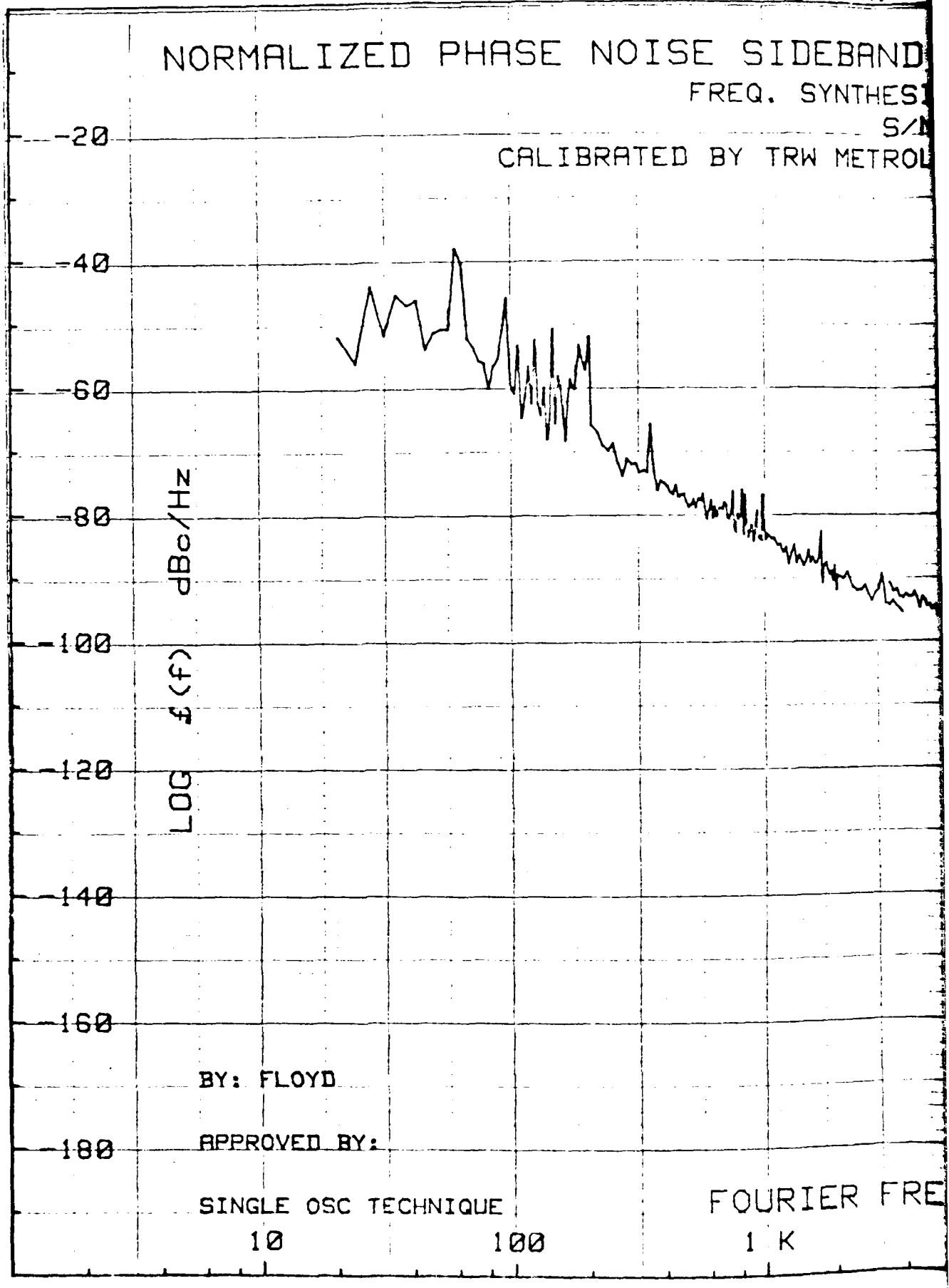
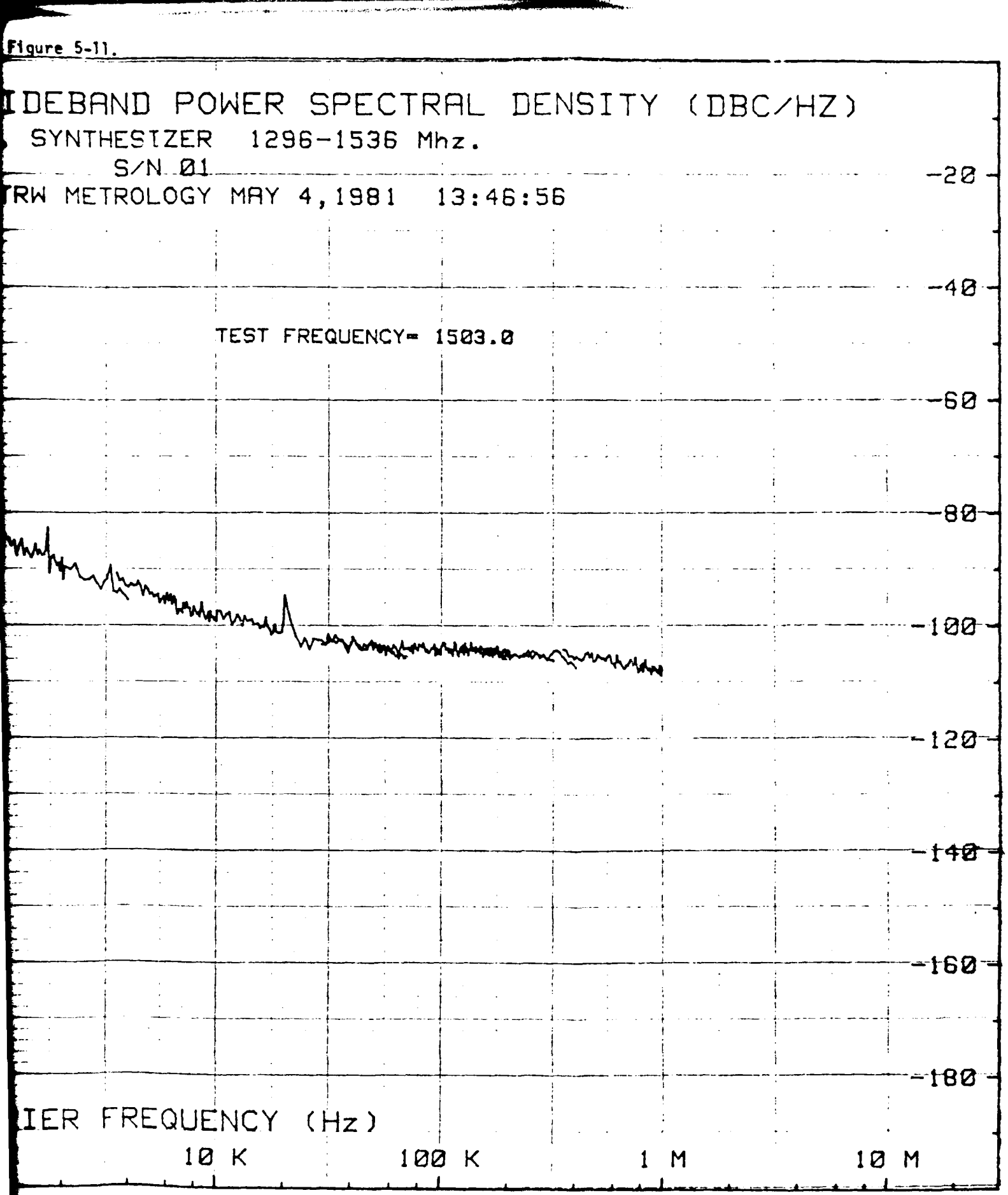

NORMALIZED PHASE NOISE SIDEBAND
FREQ. SYNTHESI
S/N
CALIBRATED BY TRW METROL
-20
-40
-60
-80
-100
-120
-140
-160
-180
LOG £(f) dBc/Hz
BY: FLOYD
APPROVED BY:
SINGLE OSC TECHNIQUE
10
100
1 K
FOURIER FRE

Figure 5-11.


IDEBAND POWER SPECTRAL DENSITY (DBC/HZ)
SYNTHESIZER 1296-1536 Mhz.
S/N 01
TRW METROLOGY MAY 4,1981 13:46:56
TEST FREQUENCY= 1503.0
-20
-40
-60
-80
-100
-120
-140
-160
-180
IER FREQUENCY (Hz)
10 K
100 K
1 M
10 M

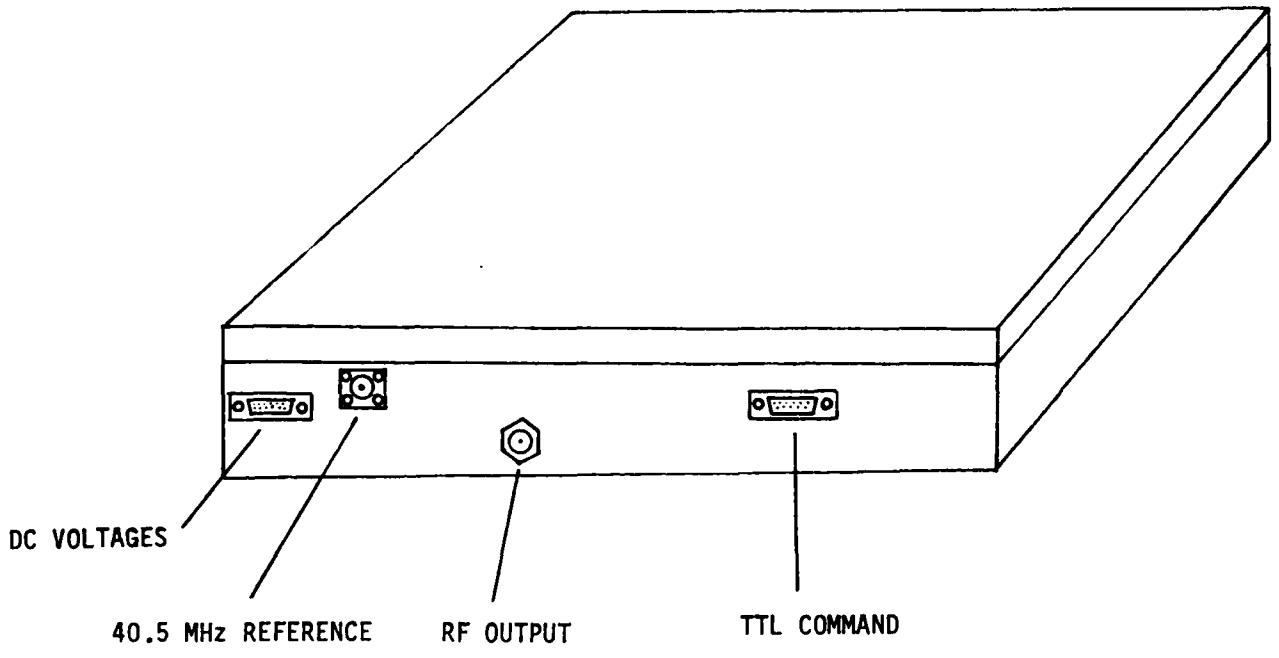


Figure 5-12. DELIVERABLE SYNTHESIZER

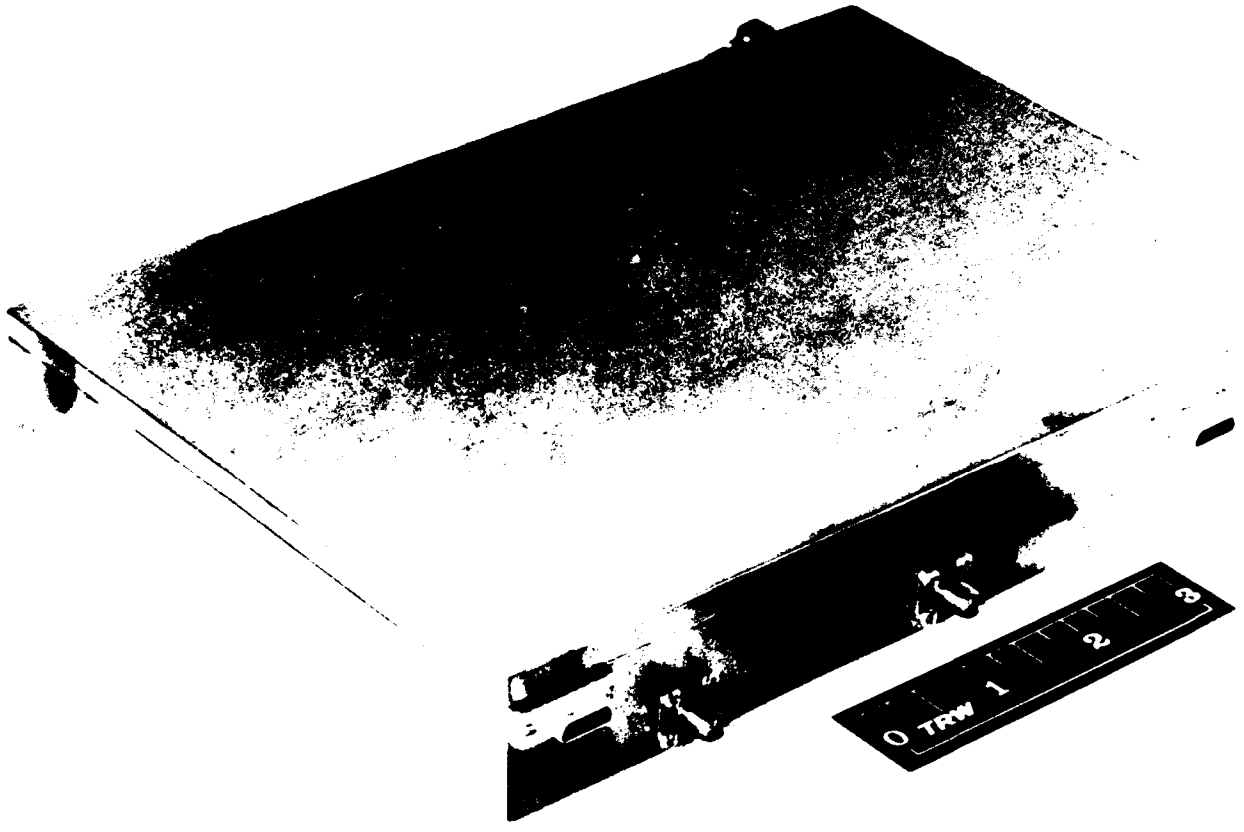


Figure 5-13. SINGLE OUTPUT DELIVERABLE SYNTHESIZER

6.0 CONCLUSIONS AND RECOMMENDATIONS

The primary objective of this program was to establish the feasibility of designing a manportable frequency synthesizer compatible with fast frequency hopped communications such as JTIDS. Key items addressed included performance parameters such as: switching speed, frequency step size, achievable bandwidth and maximum suppression of spurious modes. The adopted design concept incorporated Surface Acoustic Wave (SAW) oscillator circuitry and demonstrated attainment of key performance parameters in a configuration which lends itself to Hybrid-LSI microelectronic packaging techniques.

TRW's approach to the task incorporated RF-LSI and SAW devices in a direct mix-and-divide architecture, while the adopted packaging concept attempted to address many of the problems associated with manufacturing a product consistent with minimization of cost, size, and weight factors. The results of this program have demonstrated the feasibility of producing a direct frequency synthesis module capable of multiple step size operation, the capabilities of which could be expanded to provide programmable step size-frequency range operation. Multi-layer PC board and RF-LSI packaging techniques were employed for further reductions in module size and weight. The majority of the program goals were attained. In some areas such as switching speed performance, the state-of-the-art was significantly advanced in producing fast-hopping frequency synthesizres.

Further improvement in performance could be achieved with additional development efforts to eliminate a number of design and packaging problems encountered with the ADM-1 circuitry but are now understood. For example, improved isolation and reduction of spurious modes could be attained through investigation of the SP3T switch-MLB interface, with possible consideration being given to an alternate multi-layer structure utilizing coplanar waveguide technology. A ceramic multi-layer medium could be incorporated for further Hybrid-LSI device utilization, as well as for its inherent high isolation characteristics.

Improvements in the hardware developed for this first-cut SAW based synthesizer effort can also be made; in fact, if additional efforts are undertaken, we are confident that development of a new era of spread spectrum communications and EW surveillance applications for the defense community would result.

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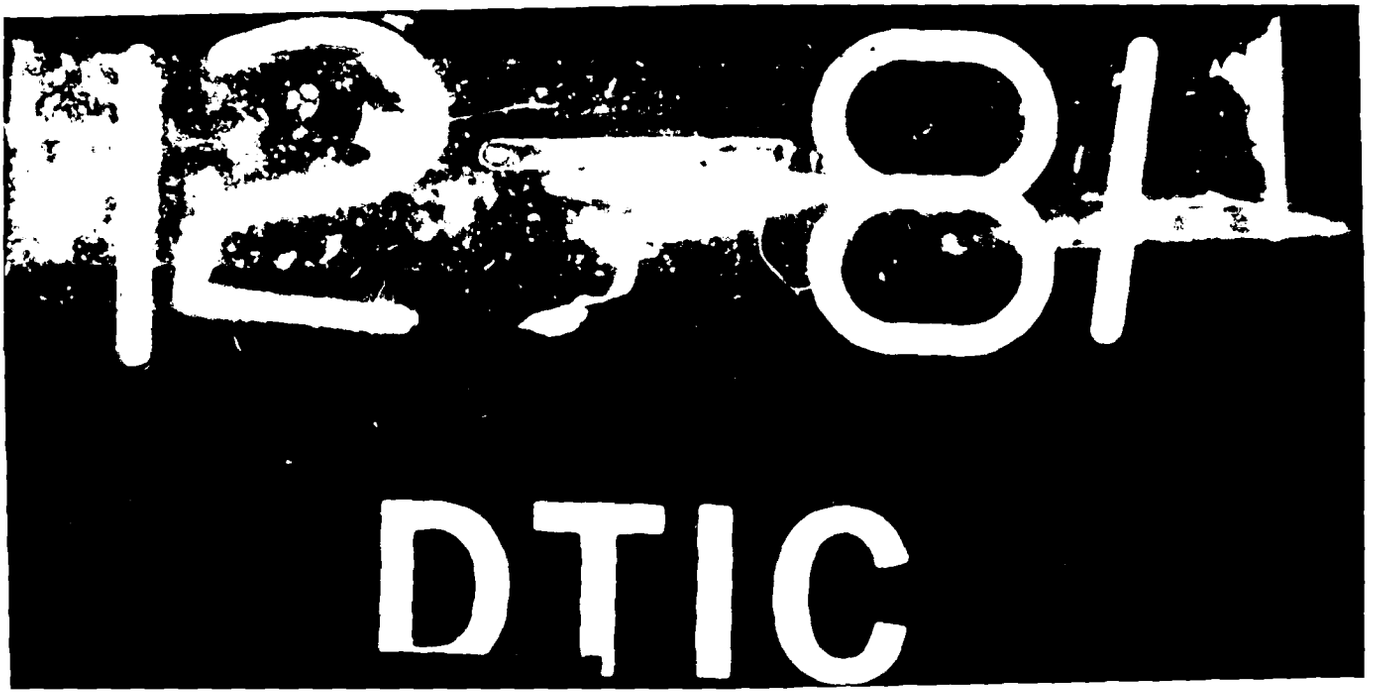
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